Silver Spur
Electronic Communications Co.

MODIFICATION INSTRUCTIONS
FOR 50 X 30 VIDEO
CHALLENGER 1P

Price includes royalty to
Mr. Steven Chalfin

INTRODUCTION:

The CHALLENGER IP (SUPERBOARD II) computer system is one of the best values in hobby computers today. Its many outstanding features are well known. However, its low price has necessitated several design compromises. One of these compromises involves the video display circuitry. The advertised 32x32 format is actually only 24x24 or at best 26x26 on a standard television. Even if a high quality monitor is used and the display size can be increased, the BASIC in ROM will still limit the line length to 24 characters.

Adding guard band circuitry would give a true 32x32 display on a standard television, but would be both expensive and technically difficult to implement. The most cost-effective solution this author has found, and the one which is described in this manual, is outlined below:

1) Double the dot clock frequency. This has the effect of putting out twice as many dots per scan line (twice as many characters per line).

2) Since there will be twice as many characters per line but the same number of lines on the screen, an additional 1K of video memory must be added.

3) Associated circuit changes for memory decoding, sync pulses, etc.

4) A software patch so that BASIC will use the entire screen to display.

These modifications yield a 32 line x 64 character display. Since this circuitry still lacks guard band capability, some characters are lost off the screen due to overscan. However, the resultant 30 line x 50 character display is a vast improvement.

It is assumed that the person undertaking this conversion is familiar with such basic electronic construction techniques as soldering and reading schematics. Components required forthis conversion are:

QUAN	DESCRIPTION
4	2114 or 2114L 450nS or faster RAM*
1	8.0 MHz crystal
1	74LS163 or 74LS161 4 bit binary counter+
1	74LS139 2 to 4 decoder (dual)+
2	16 pin DIP sockets

*This is critical! Don't buy slower (cheaper) RAMs as they will not work.

+Be sure to use the 74LS series, not the 74 series as these are slower and may not work.

Also required: Model 600 schematic, solder, #30 AWG wire wrap wire, soldering iron, wire stripper, razor blade or X-acto knife.

These parts may be had for $40 or less, depending on how well stocked your junk box is.

STARTING ON THE RIGHT FOOT:

Unless you have absolute confidence in the quality control procedures of IC manufacturers you should test the parts which will be used in this conversion. The easiest way to do this is simply to substitute them for equivalent parts on the 600 board.

First, remove the six screws securing the bottom of the case. Then remove the six screws securing the 600 board to the top of the case. Carefully unplug the power and interface connectors and place the board on a clean work surface, component side up. Carefully remove U57 and replace it with your new 74LS163. Carefully remove U17 and replace it with your new 74LS139.

Carefully remove the video RAMs (U39, U40), which will not be used in the new circuitry, and replace with 2 of the new 2114's. Recheck the orientation of the new chips. Reconnect the 600 board. Turn on the power. Try reading programs by cassette, printing on the screen, etc. to make sure everthing is working. Run a memory test program on the video RAM space 53248-54272 decimal or D000 to D3FF hex. A short, but slow program is shown below:

```
10 FOR I=53248TO54272:FOR J=0TO255
20 POKEI,J:IF PEEK(I)<>JTHENSTOP
30 NEXT:NEXTI
40 ?"OK"
```

BREAK IN 20 indicates a memory read or write error. If everything looks good remove the board again and replace the two new video RAMs with the two remaining new 2114's. Reinstall the board and rerun the memory test program. If everything checks out remove the board once again.

SPEEDING UP THE CLOCK:

Unsolder the crystal, X1. Install in its place the new 8.0 MHz crystal. Be sure to bend the leads so that the crystal is flat against the board.

This doubles the frequency of all clock lines on the board: CLK, C0-C15, $\emptyset 0_{in}$, VS, HS, TxCLK. Since the microprocessor used in the CIP is a 6502A, which is rated to run at 2.0 MHz, this modification will also double the speed of your computer. The author has some reservations about running the CIP at 2 MHz, as this speed may be pushing the system RAMs (550nS) at their limit. The author's system has been running at this speed for over 150 hours with no apparent read or write errors, but in anticipation of individual variations in different CIP's a modification to return the speed to 1 MHz will be given.

MEMORY, SYNC, ETC.

The CIP uses multiplexer circuitry so that the video address lines may be connected either to the video circuitry or the system address buss. Normally, the video display memory is connected to the video circuitry. However, when the system address buss specifies an address between DØØØ and D3FF (hex), the multiplexer switches connection of the video address lines (VAØ - VA9) to the address buss.

Control of the video RAM is directed by lines: $\overline{WVE}$, $\overline{RVE}$, $\overline{MCS}$, $\overline{VA}$. Since the video RAM will be expanded to occupy addresses DØØØ - D7FF (hex) the address decoding for the above mentioned signals must be altered accordingly.

Refer to FIG 1:

1) Cut the ($\overline{A1Ø}$) trace to U2Ø pin 1.
2) Connect U2Ø pin 1 to the adjacent Vcc buss.
3) Cut the ($\overline{WKB}$) trace to U2Ø pin 11.
4) Connect the previously cut ($\overline{WKB}$) trace to U2Ø pin 10.
5) Cut the ($\overline{RKB}$) trace at the point shown, where it runs next to the GND buss.
6) Connect the previously out ($\overline{RKG}$) trace to U2Ø pin 14.

Be sure that all cut traces are cut all the way through. An easy way to do this is to make two parallel cuts across the trace approximately 1/16th of an inch apart. Then, with the point of your blade, scrape off the small piece between the cuts.

Also, try to keep your wires as short and direct as possible.

Refer to FIG 2:

7) Cut the ($\overline{A10}$) trace on the component side of the board at the plated through hole, where it emerges just under the rightmost prototyping area (U26).

Not shown:

8) Connect U56 pin 1 and U56 pin 2 together on the foil side of the board.

Refer to FIG 3:

9) Cut the (C7) trace from U59 pin 11 at the plated through hole on the component side of the board as shown just above and to the left of U59.

10) Cut the (C11) trace from U54 pin 6 at the plated through hole just above U54, as shown.

Refer to FIG 4:

11) Cut the (GND) trace to U55 pin 10 on the foil side of the board.

12) Cut the ($\overline{\text{Ø2}}$) trace where it runs next to the GND buss just above U41, the character generator ROM.

13) Solder two 16 pin DIP sockest in the two rightmost prototyping areas (U26, U27).

14) Connect U26 pin 8 to the GND buss. Connect U26 pin 16 to the Vcc buss.

15) Connect U27 pin 8 to the GND buss. Connect U27 pin 1 to the Vcc buss.

16) Using short pieces of wire, connect U26 pins 3, 8, 14, and 15 together.

17) Using short pieces of wire, connect U27 pins 3, 4, 5, 6, and 8 together.

18) Connect the previsouly cut ($\overline{\text{Ø2}}$) trace to U26 pin 1, as shown.

19) Connect U55 pin 10 to U26 pin 12.

20) Connect U55 pin 11 to U26 pin 5.

21) Connect U55 pin 13 to U26 pin 10.

22) Connect U55 pin 14 to U26 pin 4.

23) Connect U26 pin 2 to the ($\overline{\text{A10}}$) trace which runs directly below the Vcc buss under U26, as shown.

24) Connect U26 pin 13 to U27 pin 14.

25) Connect U27 pins 9 and 16 together and to the Vcc buss directly under U27.

26) Connect U27 pin 10 to U 61 pin 15.

27) Connect U27 pin 2 to U30 pin 2.

28) Connect U27 pin 14 to U65 pin 1.

29) Connect U27 pin 7 to U30 pin 15.

30) Connect U60 pin 14 to U54 pin 6.

31) Connect U60 pin 14 to the trace which runs directly below the topmost Vcc buss on the board, as shown.

32) Connect U41 pin 6 to the (C11) trace which runs between the two plated through holes above U54, as shown.

33) Cut the (C4) trace which runs just above the GND buss over U54, as shown.

34) Connect the previously cut (C4) trace to U59 pin 13.

Refer to FIG 5:

35) Cut the three (C10), (C9), (C8) traces to U41 pins 6, 7, and 8.

36) Connect the middile (C9) trace to U41 pin 8.

37) Connect the right (C10) trace to U41 pin 7. Leave the left (C8 trace unconnected.

Refer to FIG 6:

38) Making very sure to correctly orient them in the same direction, piggy-back two fo the new 2114L memory chips as shown. Be absolutely certain that all pins of the top chip are in contact with the corresponding pins on the lower chip, except pin 8. Bend pin 8 of the upper chip away from pin 8 of the lower chip.

    Solder a 6" length of ww wire to pin 8 of the upper chip as shown.

39) Repeat step (38) for the remaining two new 2114L's.

40) Making sure they are oriented correctly, insert the two piggybacked 2114L assemblies into sockets U29 and U40.

41) Route the two wires from pin 8 through the nearest plated through holes to the foil side of the board and connect them to U55 pin 12.

42) Insert the 74LS139 into socket U26. Be sure orientation is correct.

43) Insert the 74LS163 into socket U27. Be sure orientation is correct.

This completes the hardware modifications to your CIP. Recheck all connections to insure they are correct. Make especially sure that pin 8 of the upper and lower 2114L's do not touch.

Reinstall the circuit the circuitboard and reconnect the power and interface connectors. Turn on the television and then the CIP. The screen should fill with random characters. Some adjustment of Horiz, Vert, Bright, and Cont may be necessary to obtain the best picture.

If the screen remains dark or if standard characters are not seen, remove power immediately and recheck all wiring.

Best picture quality and the most characters per line are obtained by direct connection of the CIP video signal to your television's video amplifier stage. This bypasses the sound trap and some of the lower bandwidth sections of the television. This modification is described in many computer magazines and will not be covered here. Also, try decreasing the low voltage control of your set as this may allow you to fit more characters per line.

Software:

The subroutine which runs the video display on the CIP is located in BASIC ROM 4, at address BF2D (hex). Since OSI uses this ROM in several of their computers, the subroutine relies on parameters located in the monitor PROM to determine the number of characters per line. These are as follows:

LOCATION	VALUES	FUNCTION
FFEØ	65	Position of cursor after CR, LF.
FFE1	17	Characters per line - 1.
FFE2	ØØ	Video memory size. (ØØ = 1K, any other number = 2K).

If one has the capability to program PROMs, the most elegant way to reset the display parameters is to simply program a duplicate monitor ROM, changing as necessary the above three addresses. Most of us, however, lack this capability and must resort to a software patch. The patch given below is essentially the same as teh BASIC subroutine, but since it is in RAM, the length, cursor position etc. may be user specified. In addition, it contains a machine language screen clear function so that a ?CHR$(1) will give a fast screen clear.

This is a fairly long patch, and storing it in RAM via the monitor is prohibitively time consuming. I would therefore recommened that you save it on tape in monitor loadable format the first time you load it and are sure all is well. A good program for saving machine code programs on tape may be found in the April, 1979 issue of MICRO magazine. When placed on tape in this format, the patch takes only 19 seconds to load.

In order for this patch to work the output vector, located at Ø21A and Ø21B (hex) must be changed from FF69 to Ø222, the start address of the patch. It should be noted that this vector is reset to FF69 every time the reset key is pressed, so a reset will necessitate reloading it with Ø222. A nice feature to minimize the amount of keyboard entry is to modify the aforementioned machine language save program to output .BD11G after the patch. This will obviate the need to reset and reload the patch start address into the output vector and will automatically cold start BASIC.

This patch is relocatable, although it will require some changes. I recommend leaving it at Ø222 as this area in RAM is not used by BASIC.

With this patch in operation, the video display will consist of 30 lines (2 are lost off the top edge of the screen) by 50 to 52 characters (12 to 14 are lost in overscan).

PATCH:

```
Ø222    8D Ø2 Ø2     STA Ø2Ø2
Ø225    48           PHA
Ø226    8A           TXA
Ø227    48           PHA
Ø228    98           TYA
Ø229    48           PHA
Ø22A    AD Ø2 Ø2     LDA Ø2Ø2
Ø22D    FØ 4C        BEQ 4C
Ø22F    AC Ø6 Ø2     LDY Ø2Ø6
Ø232    FØ Ø8        BEQ Ø8
Ø234    A2 4Ø        LDX 4Ø
Ø236    CA           DEX
Ø237    DØ           BNE FD
Ø239    FD           DEY
Ø23A    88           BNE F8
Ø23C    DØ F8        CMP ØA       Linefeed?
Ø23E    C9 ØAFØ 46   BEQ 46
Ø24Ø    C9 Ø1        CMP Ø1       Screen clear?
Ø242    DØ 1A        BNE 1A
Ø244    A9 2Ø        LDA 2Ø       Screen clear subroutine.
Ø246    AØ Ø8        LDY Ø8
Ø248    A2 ØØ        LDX ØØ
Ø24A    9D ØØ DØ     STAX DØØØ
Ø24D    E8           INX
Ø24E    DØ FA        BNE FA
Ø25Ø    EE 4C Ø2     INC DØ
Ø253    88           DEY
Ø254    DØ F4        BNE F4
Ø256    A9 DØ        LDA DØ
Ø258    8D 4C Ø2     STA Ø24C
Ø25B    4C 7B Ø2     JMP Ø27B
Ø25E    C9 ØD        CMP ØD       Carriage Return?
Ø26Ø    DØ Ø6        BNE Ø6
Ø262    2Ø D2 Ø2     JSR Ø2D2
Ø265    4C 7B Ø2     JMP Ø27B
Ø268    8D Ø1 Ø2     STA Ø2Ø1
Ø26B    2Ø C8 Ø2     JSR Ø2C8
Ø26E    EE ØØ Ø2     INC Ø2ØØ
Ø271    A9 F9        LDA F9*
Ø273    CD ØØ Ø2     CMP Ø2ØØ
Ø276    3Ø ØB        BMI ØB
Ø278    2Ø DA Ø2     JSR Ø2DA
Ø27B    68           PLA
Ø27C    A8           TAY
Ø27D    68           PLA
Ø27E    AA           TAX
Ø27F    68           PLA
Ø28Ø    4C 6C FF     JMP FF6C
```

3,932160
3,932160
7,86432Ø

```
Ø283        2Ø D5 Ø2        JSR Ø2D5
Ø286        2Ø C8 Ø2        JSR Ø2C8
Ø289        A9 BF           LDA BF+
Ø28B        EA              NOP
Ø28C        EA              NOP
Ø28D        8D Ø2 Ø2        STA Ø2Ø2
Ø29Ø        A2 Ø7           LDX Ø7
Ø292        BD F3 BF        LDAX EFF3
Ø295        9D Ø7 Ø2        STAX Ø2Ø7
Ø298        CA              DEX
Ø299        1Ø F7           BPL F7
Ø29b        A2 D7           LDX D7
Ø29D        A9 4Ø           LDA 4Ø
Ø29F        8D Ø8 Ø2        STA Ø2Ø8
Ø2A2        AØ ØØ           LDY ØØ
Ø2A4        2Ø Ø7 Ø2        JSR Ø2Ø7
Ø2A7        DØ FB           BNE FB
Ø2A9        EE Ø9 Ø2        INC Ø2Ø9
Ø2AC        EE ØC Ø2        INC Ø2ØC
Ø2AF        EC Ø9 Ø2        CPX Ø2Ø9
Ø2B2        DØ FØ           BNE FØ
Ø2B4        2Ø Ø7 Ø2        JSR Ø2Ø7
Ø2B7        CC Ø2 Ø2        CPY Ø2Ø2
Ø2BA        DØ F8           BNE F8
Ø2BC        A9 2Ø           LDA 2Ø
Ø2BE        2Ø ØA Ø2        JSR Ø2ØA
Ø2C1        CE Ø8 Ø2        DEC Ø2Ø8
Ø2C4        DØ F8           BNE F8
Ø2C6        FØ AE           BEQ AE
Ø2C8        AE ØØ Ø2        LDX Ø2ØØ
Ø2CB        AD Ø1 Ø2        LDA Ø2Ø1
Ø2CE        9D ØØ D7        STAX D7ØØ
Ø2D1        6Ø              RTS
Ø2D2        2Ø C8 Ø2        JRS Ø2C8
Ø2D5        A8 C8           LDA C8#
Ø2D7        8D ØØ Ø2        STA Ø2ØØ
Ø2DA        AE ØØ Ø2        LDX Ø2ØØ
Ø2DD        BD ØØ D7        LDAX D7ØØ
Ø2EØ        8D Ø1 Ø2        STA Ø2Ø1
Ø2E3        A9 5F           LDA 5F
Ø2E5        DØ E7           BNE E7
```

Output Vector: Ø21A 22 Ø2

Code Start: .BD11 G

Warm Start: .A274 G

* Cursor starting position + no. of characters per line - 1.

\+ Cursor starting position - no. of characters lost in left overscan.

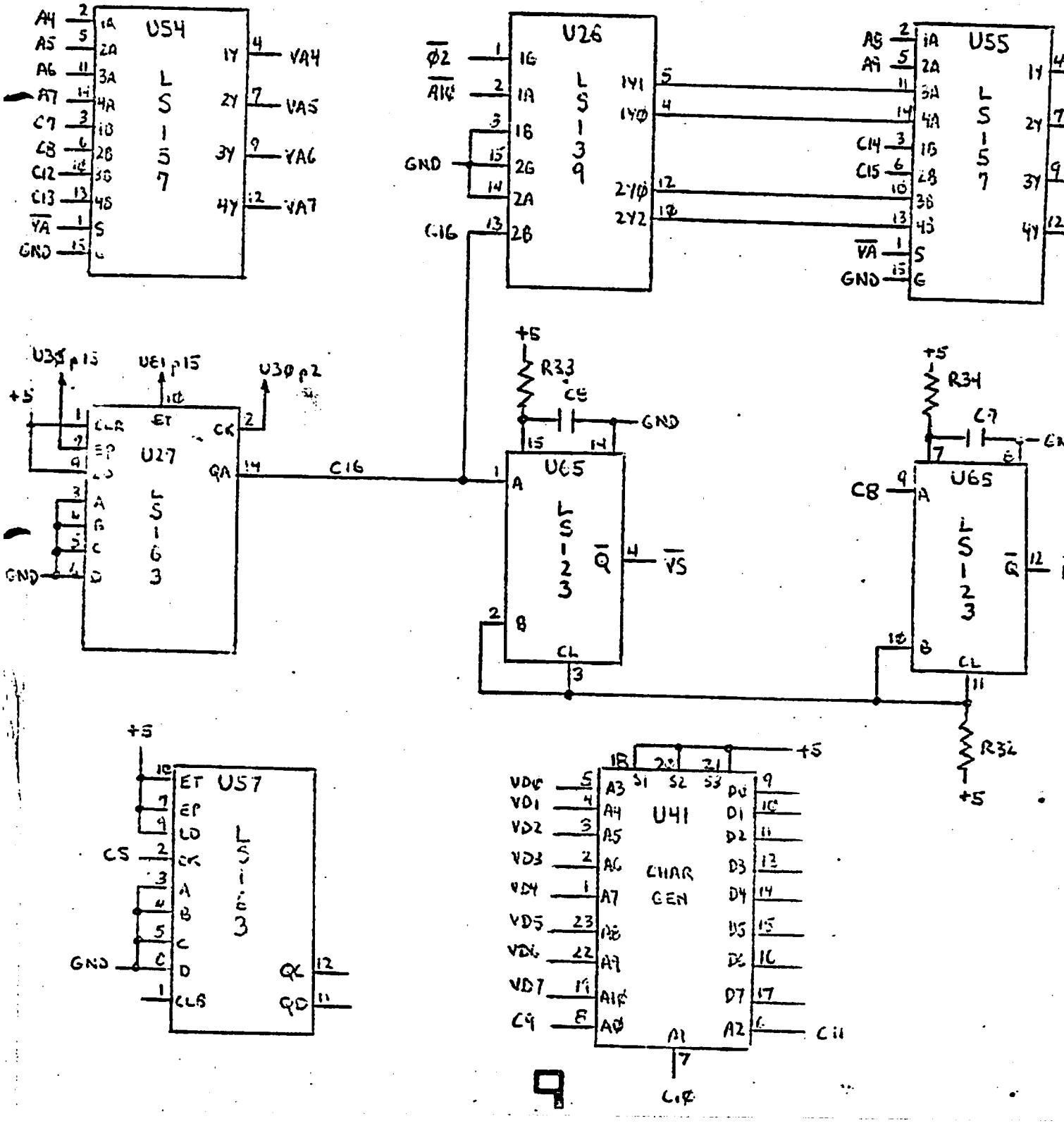
\# Cursor starting position.

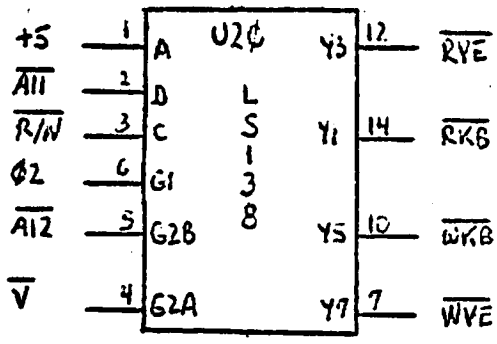
BACK TO 1MHz:

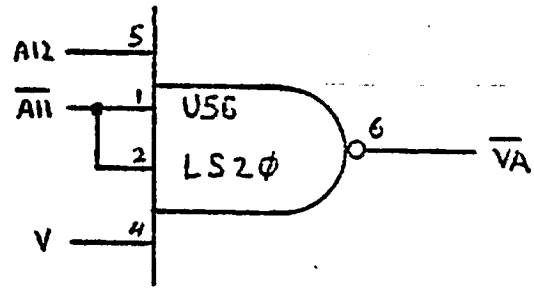
Should you find that the system RAM is not performing adequately at 2MHz, you can return the processor clock to 1 MHz by:

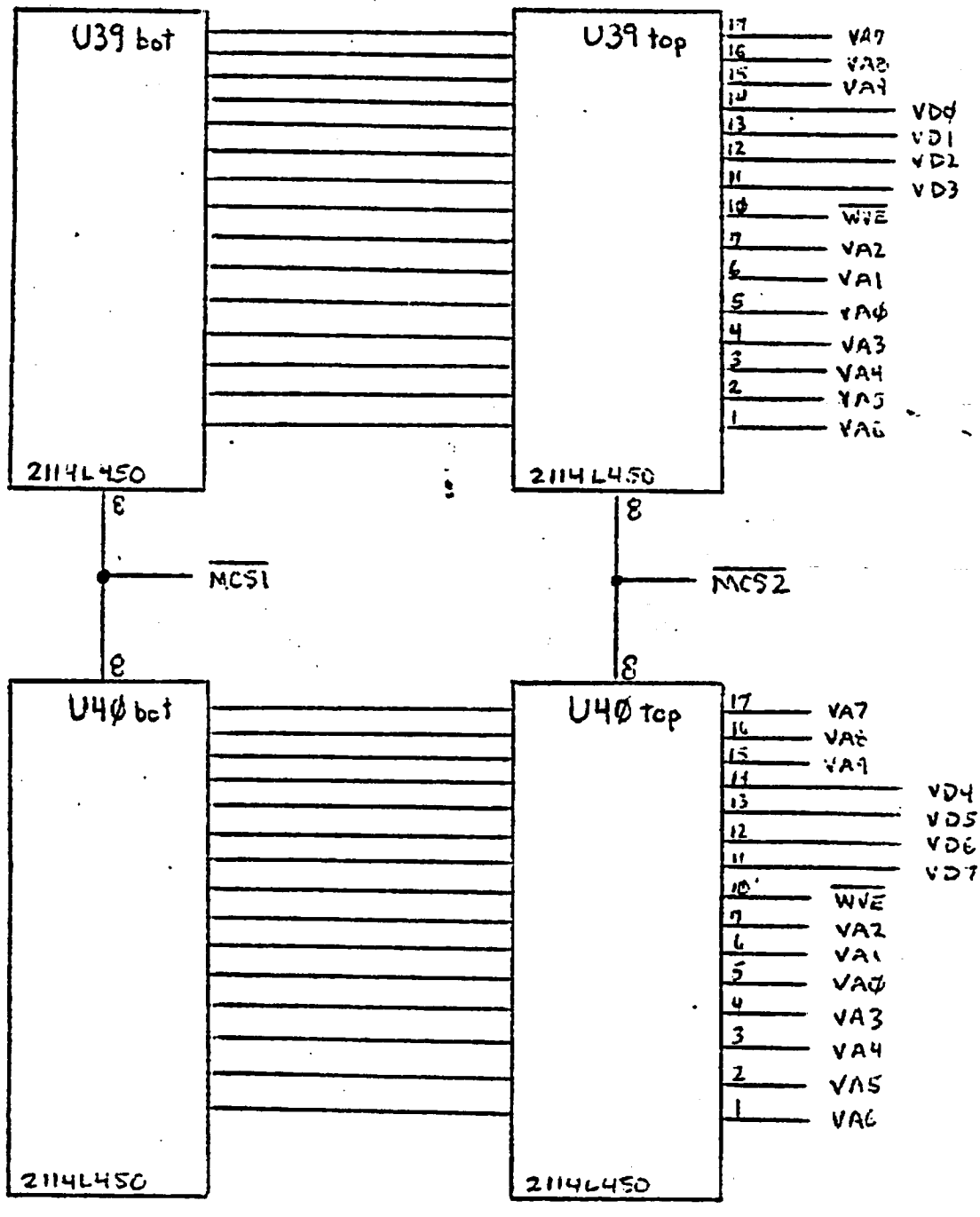
1) On the component side of the board, cut the (ØOin) trace to U3 pin 37.

2) Connect U3 pin 37 to U30 pin 12.




+5
A11
R/W
Φ2
A12
V
U2Φ
A
D
C
G1
G2B
G2A
LS138
Y3
Y1
Y5
Y7
RYE
RKB
WKB
WVE


A12
A11
V
U56
LS2Φ
VA


U39 bot
2114L450
U39 top
2114L450
VA7
VA8
VA9
VDΦ
VD1
VD2
VD3
WVE
VA2
VA1
VAΦ
VA3
VA4
VA5
VA6
MCS1
MCS2
UΦ bot
2114L450
UΦ top
2114L450
VA7
VA8
VA9
VD4
VD5
VD6
VD7
WVE
VA2
VA1
VAΦ
VA3
VA4
VA5
VA6

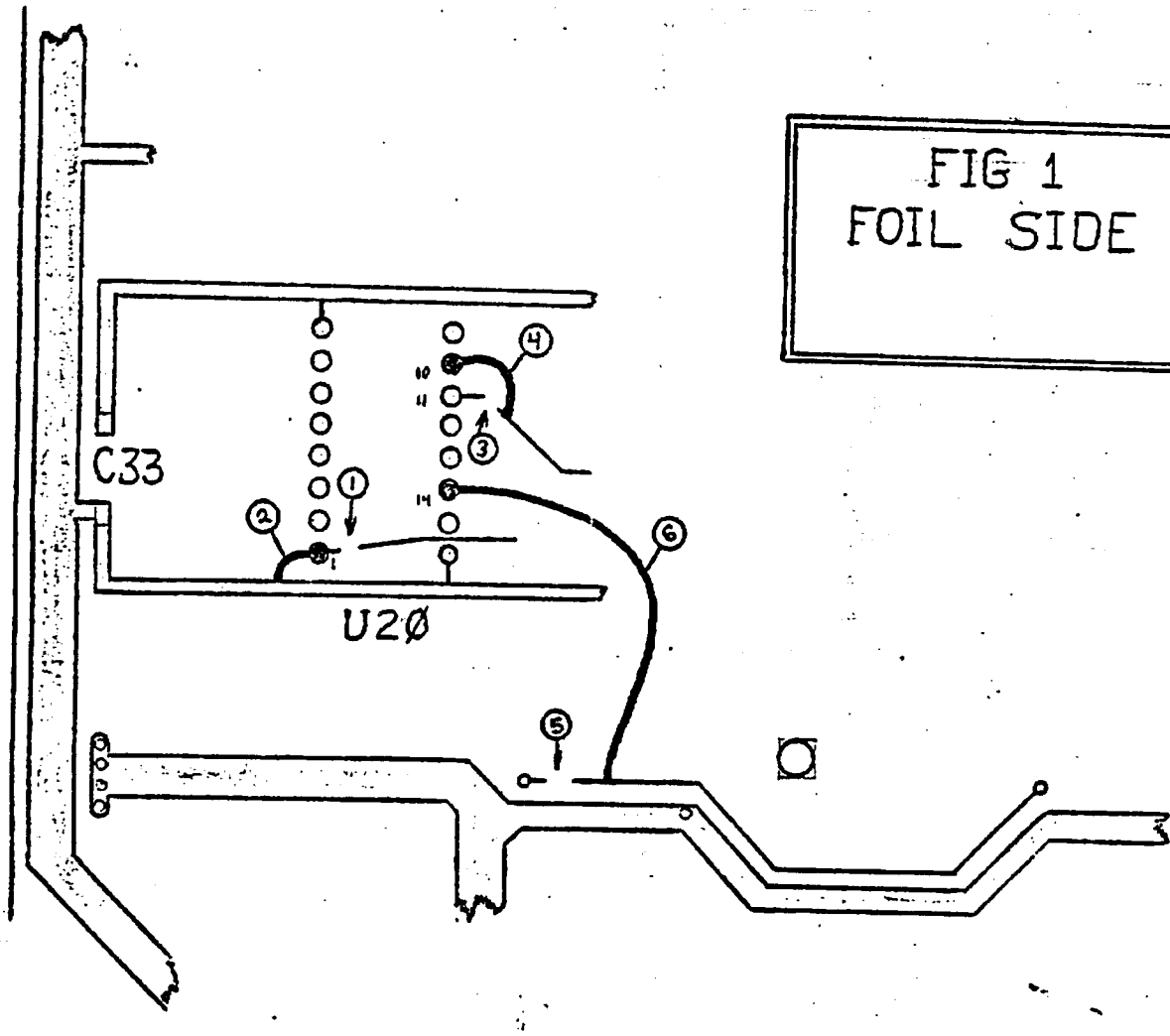


FIG 1
FOIL SIDE

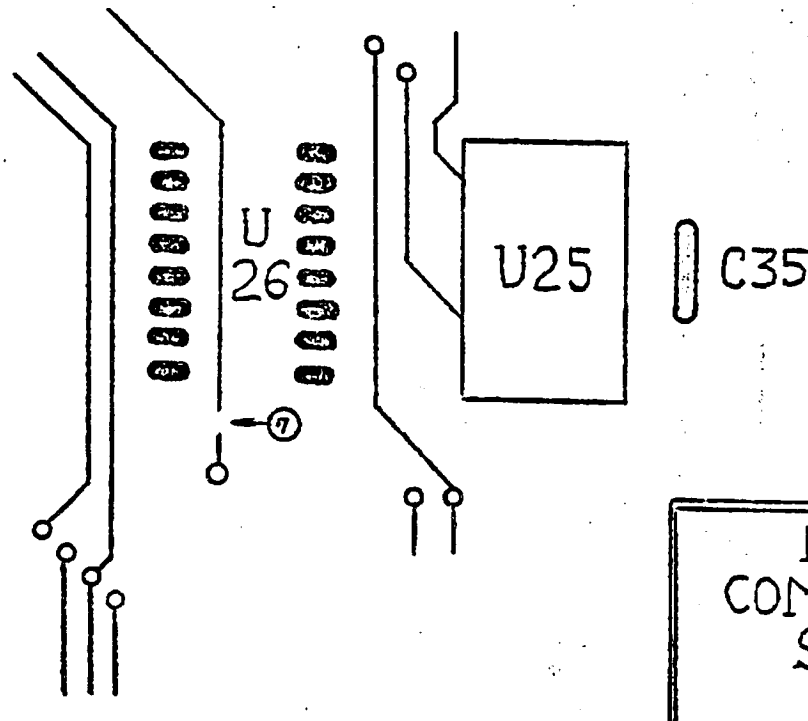


FIG 2
COMPONENT
SIDE

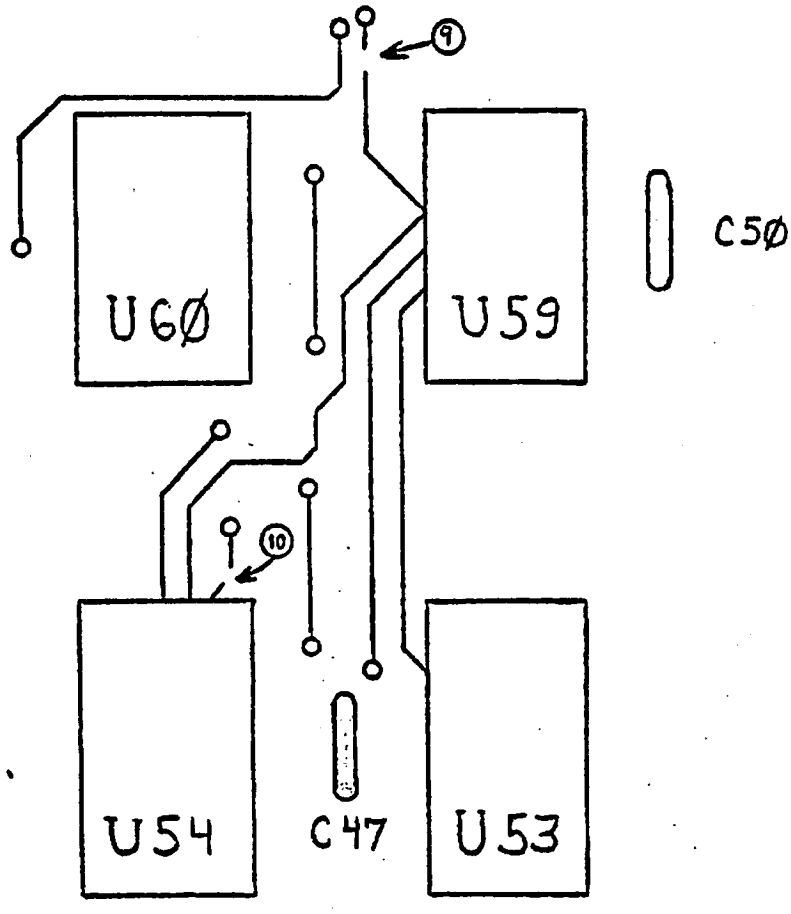
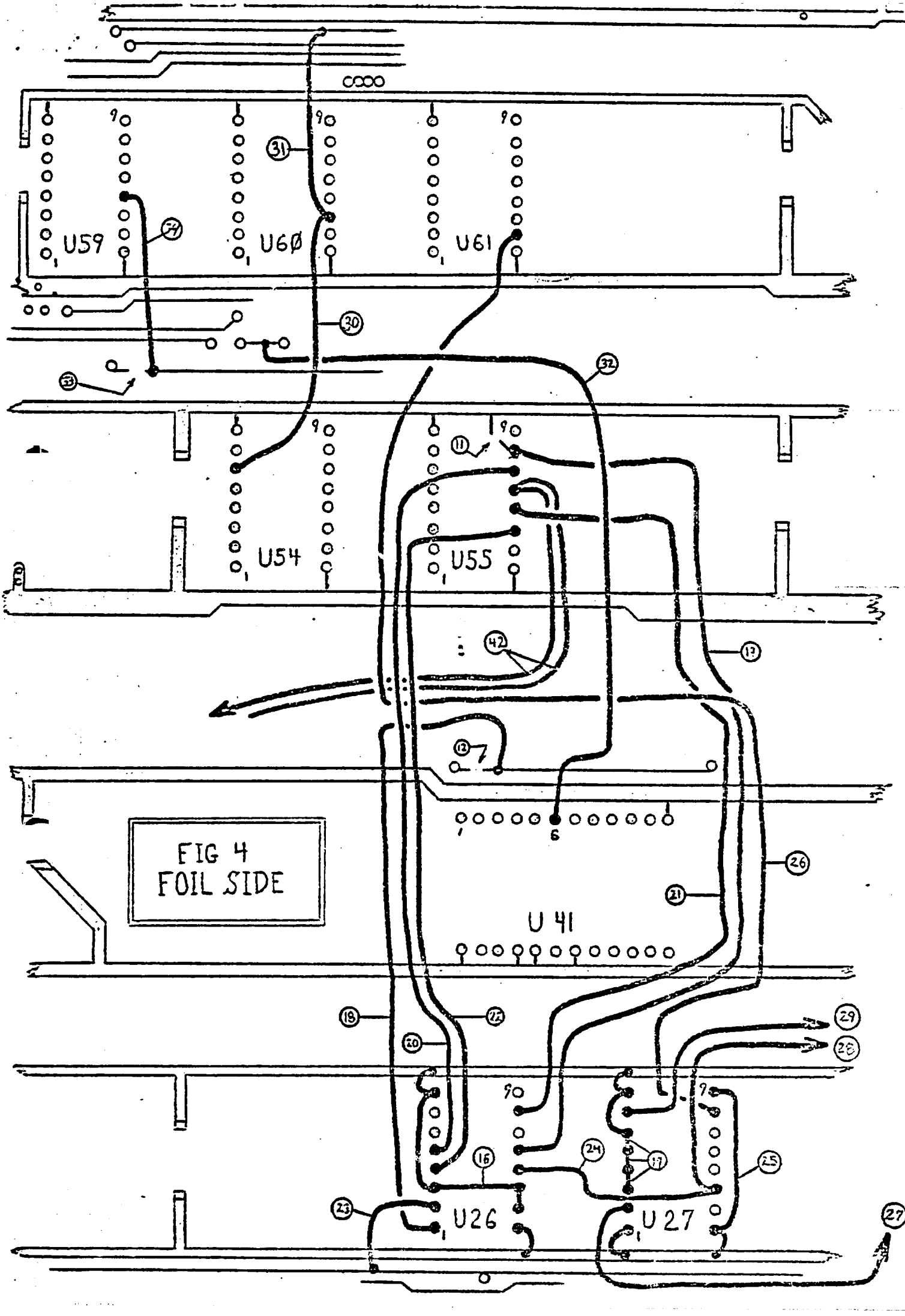


FIG 3
COMPONENT
SIDE


U59
U60
U61
U54
U55
U41
U26
U27
31
30
32
33
11
42
13
12
6
26
21
18
22
20
29
28
16
24
17
25
23
27
FIG 4
FOIL SIDE

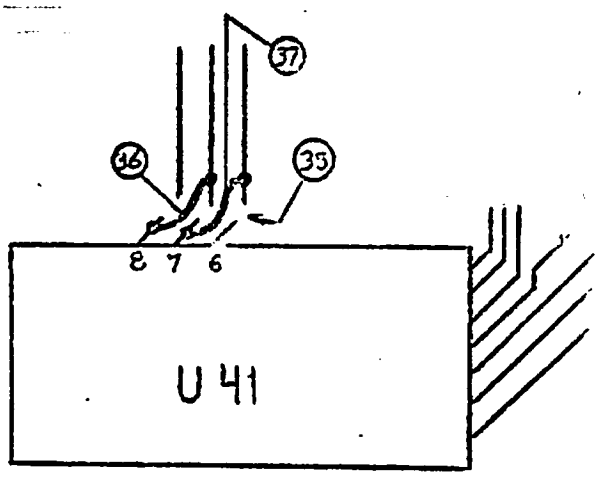


FIG 5
COMPONENT SIDE

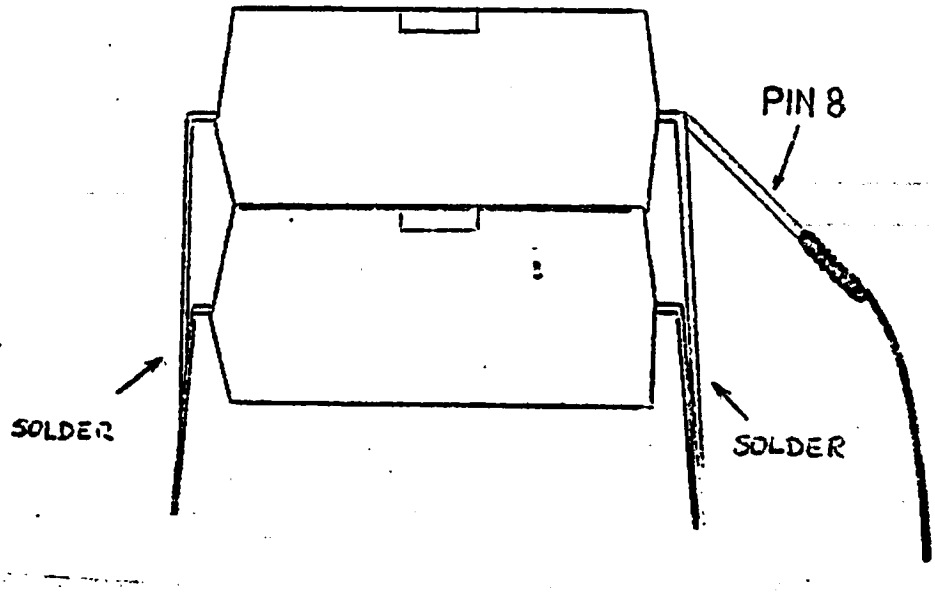


FIG 6

ERRATA :

Please add the following step

Cut the (C15) trace to U65 pin 1 at that pin.