Low Voltage Logic Interfacing

INTRODUCTION

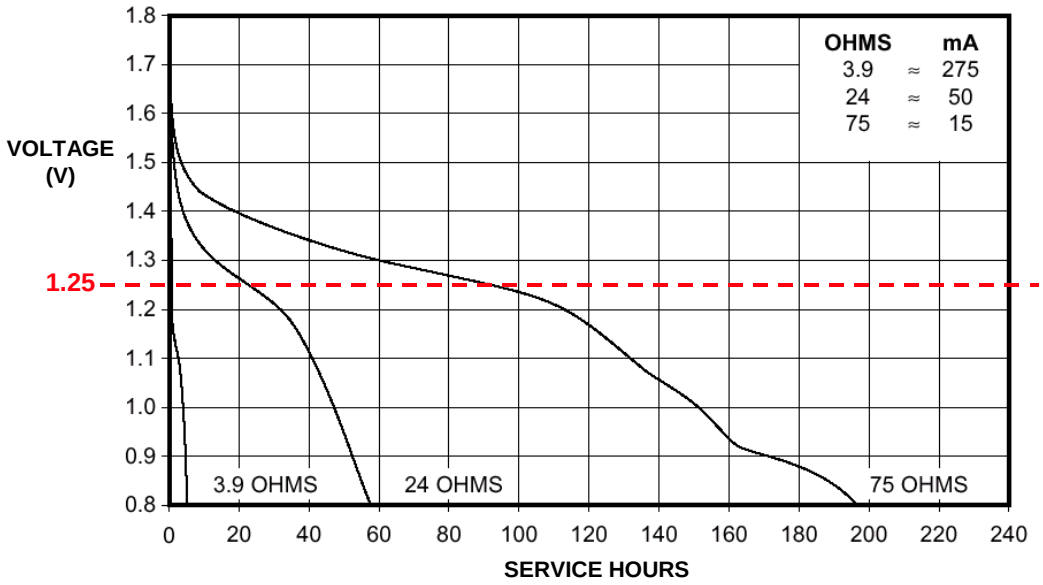
For nearly 20 years, the standard V_{DD} for digital circuits was 5 V. This voltage level was used because bipolar transistor technology required 5 V to allow headroom for proper operation. However, in the late 1980s, Complimentary Metal Oxide Semiconductor (CMOS) became the standard for digital IC design. This process did not necessarily require the same voltage levels as TTL circuits, but the industry adopted the 5 V TTL standard logic threshold levels to maintain backward compatibility with older systems (Reference 1).

The current revolution in supply voltage reduction has been driven by demand for faster and smaller products at lower costs. This push has caused silicon geometries to drop from 2 µm in the early 1980s to 0.90 nm and 45 nm that is used in many of today's latest FPGA, microprocessor, and DSP designs. As feature sizes have become increasingly smaller, the voltage for optimum device performance has also dropped below the 5 V level. This is illustrated in the current FPGAs, microprocessors, and DSPs, where the optimum core operating voltage can be as low as 1 V or less.

The strong interest in lower voltage DSPs is clearly visible in the shifting sales percentages for 5 V and 3.3 V parts. Sales growth for 3.3 V DSPs has increased at more than twice the rate of the rest of the DSP market (30% for all DSPs versus more than 70% for 3.3 V devices). This trend will continue as the high volume/high growth portable markets demand signal processors that contain all of the traits of the lower voltage DSPs.

On the one hand, the lower voltage ICs operate at lower power, allow smaller chip areas, and higher speeds. On the other hand, the lower voltage ICs must often interface to other ICs which operate at larger V_{DD} supply voltages thereby causing interface compatibility problems. Although lower operating voltages mean smaller signal swings, and hence less switching noise, noise margins are lower for low supply voltage ICs.

The popularity of 2.5 V devices can be partially explained by their ability to operate from two AA alkaline cells. Figure 1 shows the typical discharge characteristics for a AA cell under various load conditions (Reference 2). Note that at a load current of 15 mA, the voltage remains above +1.25 V (2.5 V for two cells in series) for nearly 100 hours. Therefore, an IC that can operate effectively at low currents with a supply voltage of 2.5 V ±10% (2.25 V - 2.75 V) is very useful in portable designs.



Courtesy: Duracell, Inc., Berkshire Corporate Park, Bethel, CT 06801
http://www.duracell.com

Figure 1: Duracell MN1500 "AA" Alkaline Battery Discharge Characteristics

In order to understand the compatibility issues relating to interfacing ICs operated at different V_{DD} supplies, it is useful to first look at the structure of a typical CMOS logic stage as shown in Figure 2.

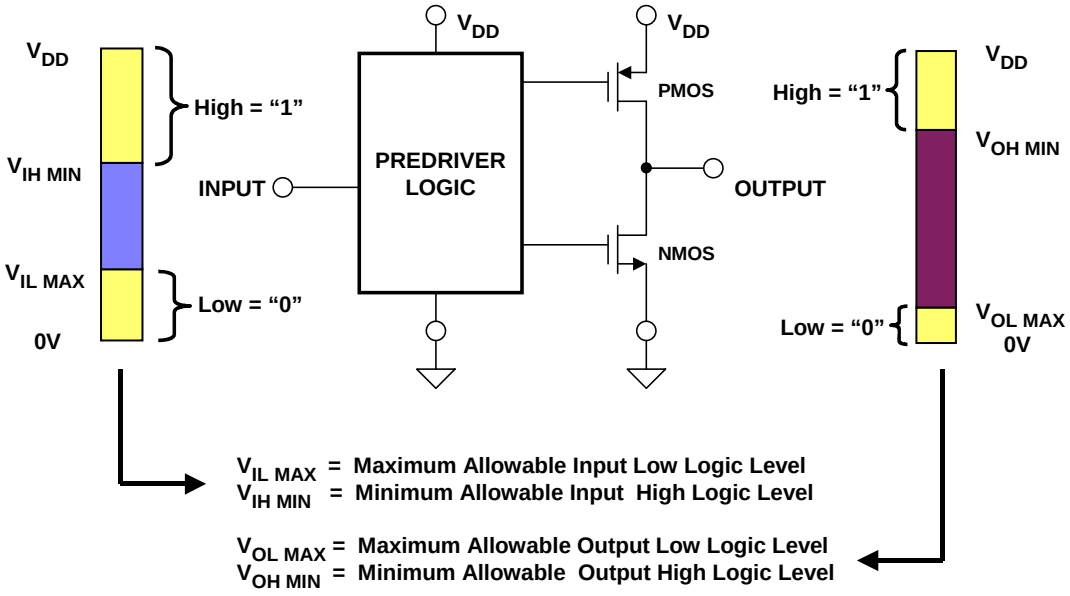


Figure 2: Typical CMOS IC Output Driver Configuration

Note that the output driver stage consists of a PMOS and an NMOS transistor. When the output is high, the PMOS transistor connects the output to the $+V_{DD}$ supply through its low on-resistance (R_{ON}), and the NMOS transistor is off. When the output is low, the NMOS transistor connects the output to ground through its on-resistance, and the PMOS transistor is off. The R_{ON} of a CMOS output stage can vary between 5 Ω and 50 Ω depending on the size of the transistors, which in turn, determines the output current drive capability.

A typical logic IC has its power supplies and grounds separated between the output drivers and the rest of the circuitry (including the pre-driver). This is done to maintain a clean power supply, which reduces the effect of noise and ground bounce on the I/O levels. This is increasingly important, since added tolerance and compliance are critical in I/O driver specifications, especially at low voltages.

Figure 2 also shows "bars" which define the minimum and maximum required input and output voltages to produce a valid high or low logic level. Note that for CMOS logic, the actual output logic levels are determined by the drive current and the R_{ON} of the transistors. For light loads, the output logic levels are very close to 0 V and $+V_{DD}$. The input logic thresholds, on the other hand, are determined by the input circuit of the IC.

There are three sections in the "input" bar. The bottom section shows the input range that is interpreted as a logic low. In the case of 5 V TTL, this range would be between 0 V and 0.8 V. The middle section shows the input voltage range where it is interpreted as neither a logic low nor a logic high. The upper section shows where an input is interpreted as a logic high. In the case of 5 V TTL, this would be between 2 V and 5 V.

Similarly, there are three sections in the "output" bar. The bottom range shows the allowable voltage for a logic low output. In the case of 5 V TTL, the IC must output a voltage between 0 V and 0.4 V. The middle section shows the voltage range that is not a valid high or low—the device should never transmit a voltage level in this region except when transitioning from one level to the other. The upper section shows the allowable voltage range for a logic high output signal. For 5 V TTL, this voltage is between 2.4 V and 5 V. The chart does not reflect a 10% overshoot/undershoot also allowed on the inputs of the logic standard.

A summary of the existing logic standards using these definitions is shown in Figure 3. Note that the input thresholds of classic CMOS logic (series-4000, for example) are defined as 0.3 V_{DD} and 0.7 V_{DD}. However, most CMOS logic circuits in use today are compatible with TTL and LVTTL levels which are the dominant 5 V and 3.3 V operating standards for DSPs. Note that 5 V TTL and 3.3 V LVTTL input and output threshold voltages are identical. The difference is the upper range for the allowable high levels.

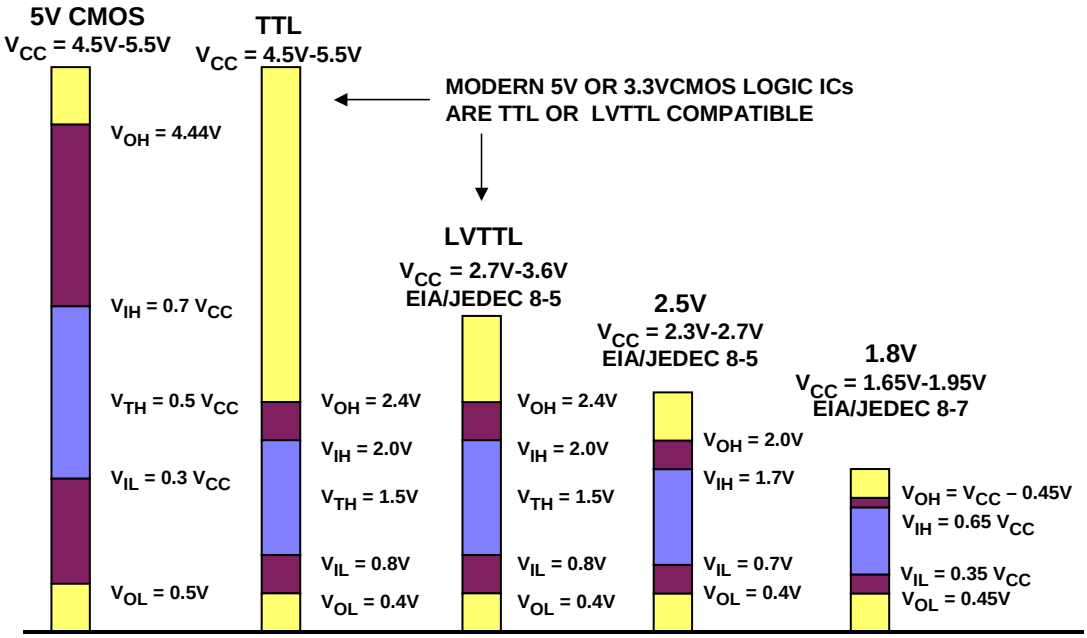


Figure 3: Standard Logic Levels

The international standards bureau JEDEC (Joint Electron Device Engineering Council) has created a 2.5 V standard (JEDEC standard 8-5) and a 1.8 V standard (Reference 3). There are also a wide range of other low voltage standards, such as GTL (Gunning Transceiver Logic), BTL (Backplane Transceiver Logic), ECL (Emitter-Coupled-Logic) PECL (Positive ECL Logic), and LVDS. However, most of these standards are aimed at application specific markets and not for general purpose semiconductor systems.

From this chart (Figure 3), it is possible to visualize some of the possible problems in connecting together two ICs operating on different standards. One example would be connecting a 5 V TTL device to a 3.3 V LVTTL IC. The 5 V TTL high level is too high for the LVTTL to handle (> 3.3 V). This could cause permanent damage to the LVTTL chip. Another possible problem would be a system with a 2.5 V IC driving a 5 V CMOS device. The logic high level from the 2.5 V device is not high enough for it to register as a logic high on the 5 V CMOS input ($V_{IH\ MIN}$ = 3.5 V). These examples illustrate two possible types of logic level incompatibilities—either a device being driven with too high a voltage or a device not driving a voltage high enough for it to register a valid high logic level with the receiving IC. These interfacing problems introduce two important concepts: *voltage tolerance* and *voltage compliance*.

VOLTAGE TOLERANCE AND VOLTAGE COMPLIANCE

A device that is *voltage tolerant* can withstand a voltage greater than its V_{DD} on its I/O pins. For example, if a device has a V_{DD} of 2.5 V and can accept inputs equal to 3.3 V and can withstand 3.3 V on its outputs, the 2.5 V device is called 3.3 V tolerant. The meaning of *input* voltage tolerance is fairly obvious, but the meaning of *output* voltage tolerance requires some explanation. The output of a 2.5 V CMOS driver in the high state appears like a small resistor

(R_{ON} of the PMOS FET) connected to 2.5 V. Obviously, connecting its output directly to 3.3 V is likely to destroy the device due to excessive current. However, if the 2.5 V device has a three-state output which is connected to a bus which is also driven by a 3.3 V IC, then the meaning becomes clearer. Even though the 2.5 V IC is in the off (third-state) condition, the 3.3 V IC can drive the bus voltage higher than 2.5 V, potentially causing damage to the 2.5 V IC output.

A device which is *voltage compliant* can receive signals from and transmit signals to a device which is operated at a voltage greater than its own V_{DD}. For example, if a device has a 2.5 V V_{DD} and can transmit and receive signals to and from a 3.3 V device, the 2.5 V device is said to be 3.3 V compliant.

The interface between the 5 V CMOS and 3.3 V LVTTL parts illustrates a lack of voltage tolerance; the LVTTL IC input is overdriven by the 5 V CMOS device output. The interface between the 2.5 V JEDEC and the 5 V CMOS part demonstrates a lack of voltage compliance; the output high level of the JEDEC IC does not comply to the input level requirement of a the 5 V CMOS device.

INTERFACING 5V SYSTEMS TO 3.3V SYSTEMS USING NMOS FET "BUS SWITCHES"

When combining ICs that operate on different voltage standards, one is often forced to add additional discrete elements to ensure voltage tolerance and compliance. In order to achieve voltage tolerance between 5 V and 3.3 V logic, for instance, a bus switch voltage translator such as the ADG3257 can be used (also see References 4, 5). The bus switch limits the voltage applied to an IC. This is done to avoid applying a larger input high voltage than the receiving device can tolerate.

As an example, it is possible to place a bus switch between a 5 V CMOS and 3.3 V LVTTL IC, and the two devices can then transmit data properly as shown in Figure 4. The bus switch is basically an NMOS FET. If 4.3 V is placed on the gate of the FET, the maximum passable signal is 3.3 V (approximately 1 V less than the gate voltage). If both input and output are below 3.3 V, the NMOS FET acts as a low resistance ($R_{ON} \approx 2\ \Omega$). As the input approaches 3.3 V, the FET on-resistance increases, thereby limiting the signal output. The ADG3257 is a quad 2:1 Mux/Demux bus switch with a gate drive enable as shown in the lower half of Figure 4. The V_{CC} of the ADG3257 sets the high level for the gate drive.

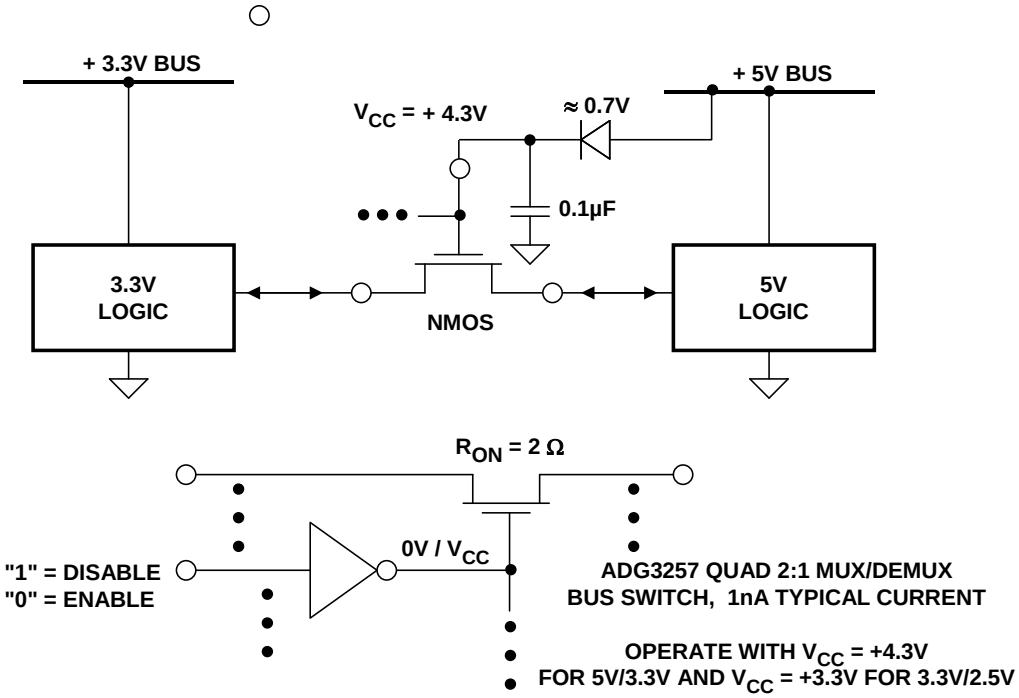


Figure 4: +5 V/+3.3 V Bidirectional Interface Using NMOS FET Achieves Voltage Tolerance

One way of creating a 4.3 V supply on a 5 V/3.3 V system board is to simply place a silicon diode between the 5 V supply and V_{CC} on the bus switch as shown in Figure 4. For 3.3 V/2.5 V applications, the V_{CC} pin can be connected directly to the +3.3 V supply. Some bus switches are designed to operate on either 3.3 V or 5 V directly and generate the internal gate bias level internally.

A bus switch removes voltage tolerance concerns in this mixed logic design. One convenient feature of bus switches is that they are bi-directional; this allows the designer to place a bus translator between two ICs and not have to create additional routing logic for input and output signals.

A bus switch increases the total power dissipation along with the total area required to layout a system. Since voltage bus switches are typically CMOS circuits, they have very low power dissipation ratings. An average value for added continuous power dissipation is 5 mW per package (10 switches), and this is independent of the frequency of signals which pass through the circuit. Bus switches typically have 8 to 20 I/O pins per package and take up approximately 25 to 50 mm^2 of board space.

One concern when adding interface logic into a circuit is a possible increase in propagation delay. Added propagation delay can create many timing problems in a design. Bus switches have very low propagation delay values.

The bus switch contributes practically no propagation delay (0.1 ns typical for the ADG3257) other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is typically much smaller than the rise/fall times of typical driving signals, bus switches add very little propagation delay to the system. Low R_{ON} is therefore critical for bus switches, since the switch on-resistance in conjunction with the bus capacitance creates a single-pole filter which can add delay and reduce the maximum data rate. The typical on-capacitance of the ADG3257 is 10 pF, and this capacitance in conjunction with an R_{ON} of 4 Ω yields a rise/fall time of approximately 90 ps. Figure 5 shows the ADG3257 on-resistance as a function of input voltage for 5.5, 5, 4.5, 3.3, 3.0, and 2.7 V supplies. Maximum pass voltage as a function of input voltage is shown in Figure 6.

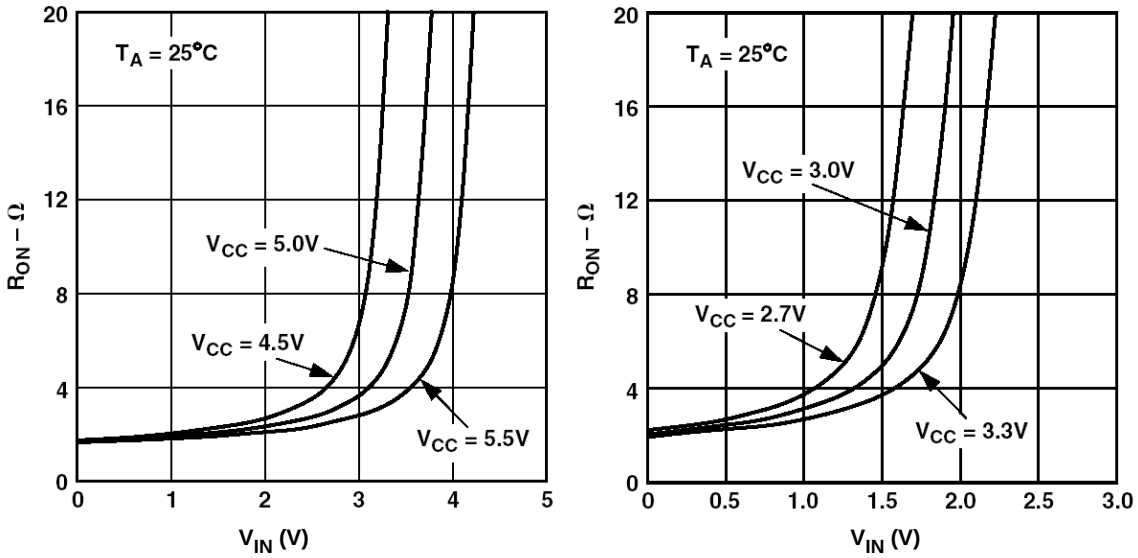


Figure 5: ON Resistance vs. Input Voltage for ADG3257 Bus Switch

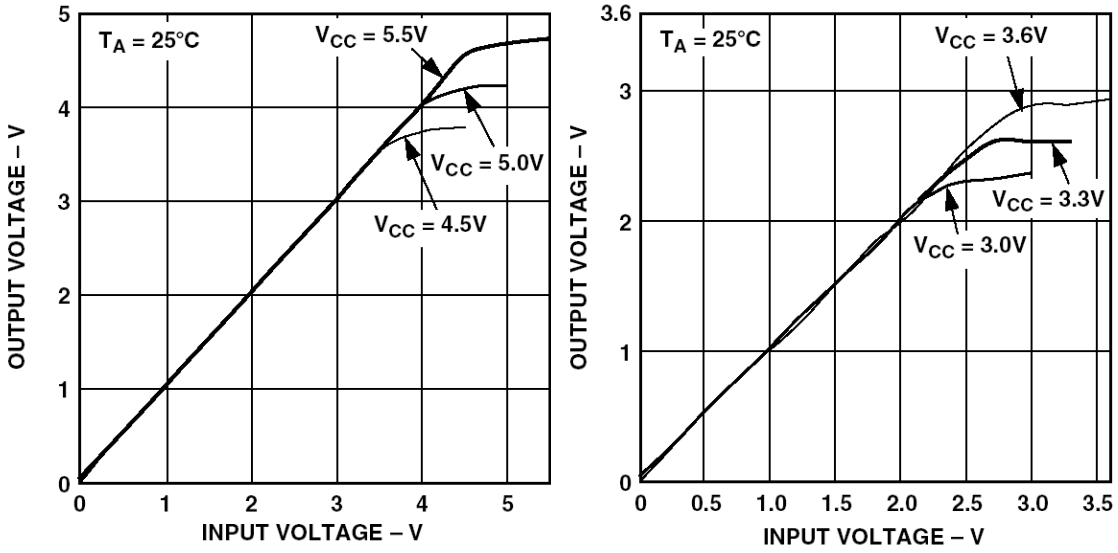


Figure 6: Maximum Pass Voltage vs. Input Voltage for ADG3257 Bus Switch

Eye diagrams for the ADG3257 operating at 622 Mbps and 933 Mbps are shown in Figure 7.

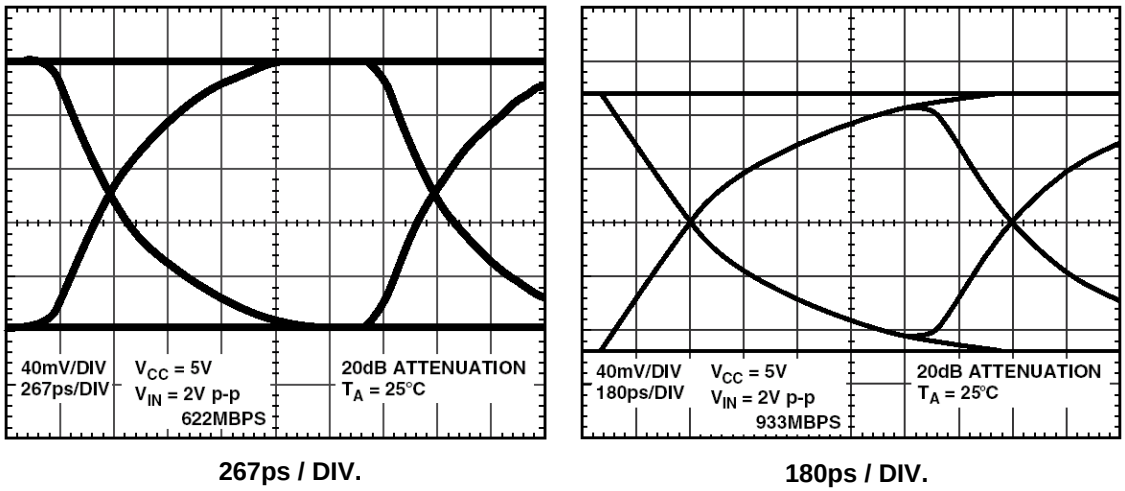


Figure 7: Eye Diagrams for 622-Mbps and 933-Mbps Data Rates

3.3V/2.5V INTERFACES

Figure 8 shows two possibilities for a 3.3 V to 2.5 V logic interface. The top diagram (A) shows a direct connection. This will work provided the 2.5 V IC is 3.3 V tolerant on its input. If the 2.5 V IC is not 3.3 V tolerant, a low-voltage bus switch such as the ADG3231 can be used. In most cases, the connection between 3.3 V and 2.5 V systems can be bi-directional, even though the V_{OH} of 2.5 V logic is specified as +2.0 V which is the same as the V_{IH} specification of 3.3 V logic (refer back to Figure 3). This point deserves further discussion.

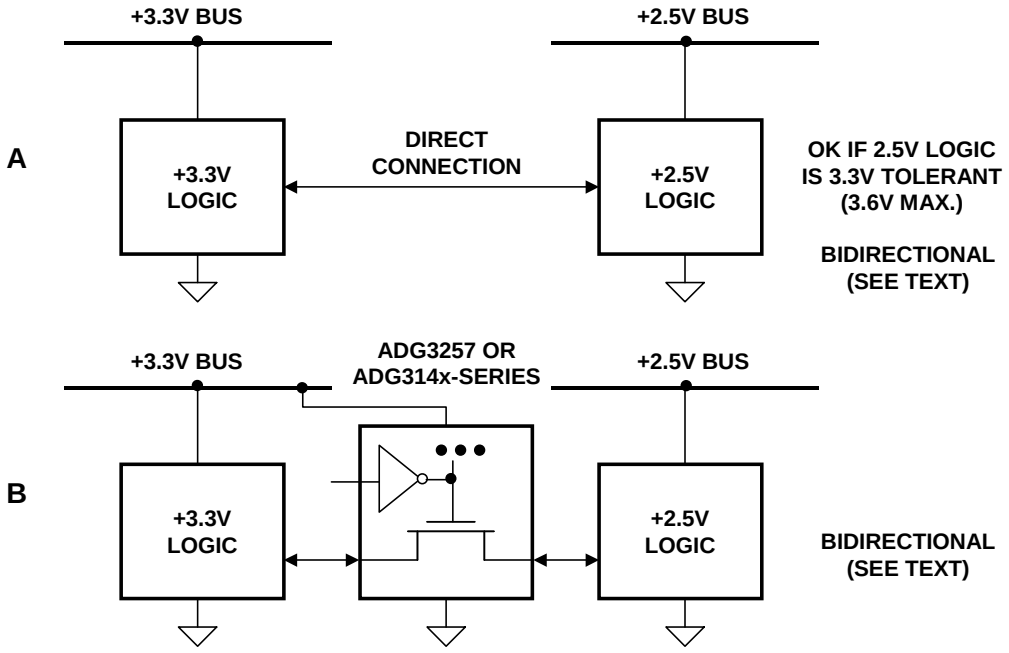


Figure 8: +3.3 V to +2.5 V Interface

Figure 9A shows a direct connection between 2.5 V and 3.3 V logic. In order for this to work, the 2.5 V output must be at least 2 V minimum per the JEDEC specifications. With no loading on the 2.5 V output, the 3.3 V IC input is connected directly to +2.5 V through the on-resistance of the PMOS transistor driver. This provides 0.5 V noise margin for the nominal supply voltage of 2.5 V. However, the tolerance on the 2.5 V bus allows it to drop to a minimum of 2.3 V, and the noise margin is reduced to 0.3 V. This may still work in a relatively quiet environment, but could be marginal if there is noise on the supply voltages.

Adding a 1.6 kΩ pull-up resistor as shown in Figure 9B ensures the 2.5 V output will not drop below 2.5 V due to the input current of the 3.3 V device, but the degraded noise margin still exists for a 2.3 V supply. With a 50% duty cycle, the resistor adds about 3.4 mW power dissipation per output.

A more reliable interface between 2.5 V and 3.3 V logic is shown in Figure 9C, where a logic translator such as the ADG3231 is used. This solves all noise margin problems associated with (A) and (B) and requires about 2 µA maximum per output.

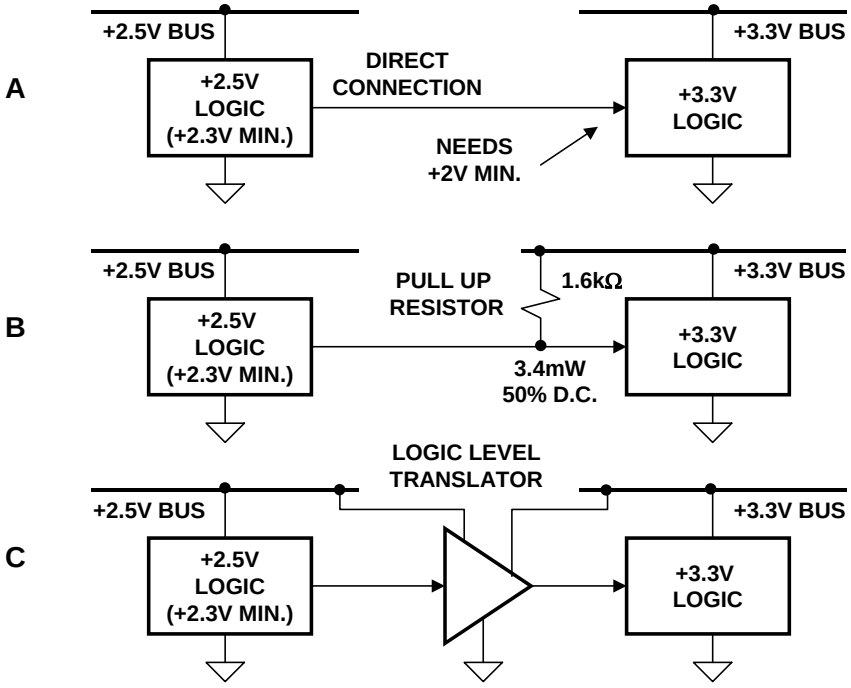


Figure 9: +2.5V to +3.3V Interface Analyzed

3.3V/2.5V, 3.3V/1.8V, 2.5V/1.8V INTERFACES

The ADG3241, ADG3242, ADG3243, ADG3245, ADG3246, ADG3247, ADG3248, and ADG3249 are low voltage bus switches optimized for operation on 3.3 V or 2.5 V supplies. The family includes 1, 2, 8, 10 and dual 8-bit switches, all of which are 2-port switches. The ADG3241, ADG3242, ADG3245, ADG3246, ADG3247, and ADG3249 have 2.5 V or 1.8 V selectable level shift capability. The family offers a fast, low-power solution for 3.3 /2.5 V,

3.3 /1.8 V, and 2.5 /1.8 V unidirectional interfaces. Figure 10 shows the ADG32xx-family used as 3.3-/1.8-V level shifters and 2.5-/1.8-V shifters.

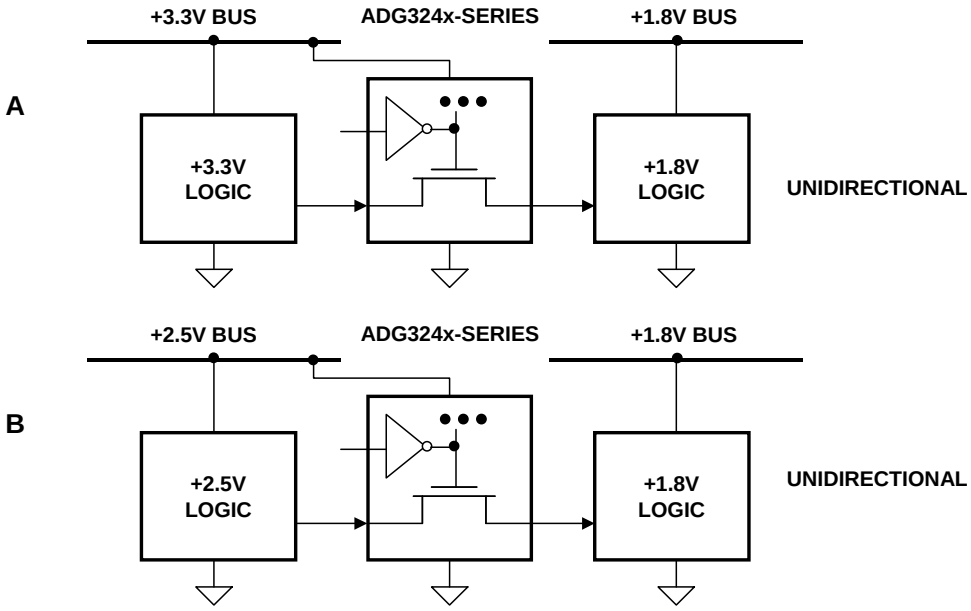


Figure 10: +3.3 V to +1.8 V, 2.5 V to +1.8 V Unidirectional Interfaces

Translating from 1.8 V to 2.5 V, 1.8 V to 3.3 V, (and sometimes 2.5 V to 3.3 V as previously discussed) requires a logic translator such as the ADG3231 shown in Figure 11. The two voltage buses can be any value between 1.65 V and 3.6 V. The ADG3231 is a single-channel translator in a SOT-23 package, and the ADG3232 is a 2:1 multiplexer/level translator also in a SOT-23 package.

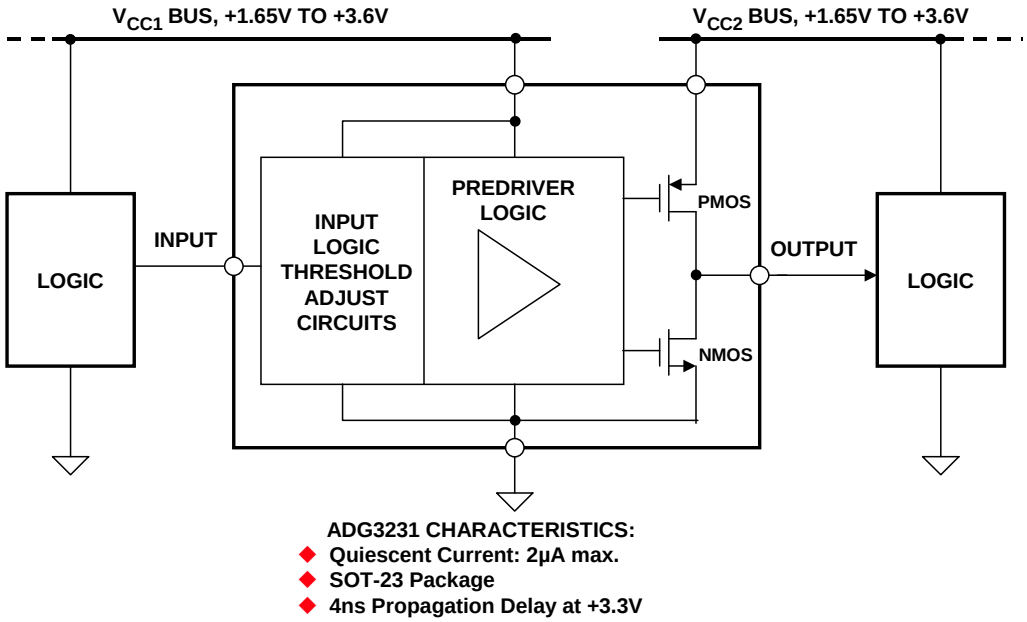


Figure 11: ADG3231 Low Voltage Logic Level Translator

The ADG3233 is a bypass switch designed on a submicron process that operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages, allowing bidirectional level translation, i.e., it translates low voltages to higher voltages and vice versa. The signal path is unidirectional, meaning data may only flow from A to Y. This type of device may be used in applications that require a bypassing function. It is ideally suited to bypassing devices in a JTAG chain or in a daisy-chain loop. One switch could be used for each device or a number of devices, thus allowing easy bypassing of one or more devices in a chain. This may be particularly useful in reducing the time overhead in testing devices in the JTAG chain or in daisy-chain applications where the user does not wish to change the settings of a particular device.

The bypass switch is packaged in two of the smallest footprints available for its required pin count. The 8-lead SOT-23 package requires only 8.26 mm × 8.26 mm board space, while the MSOP package occupies approximately 15 mm × 15 mm board area. A functional block diagram of the ADG3233 is shown in Figure 12.

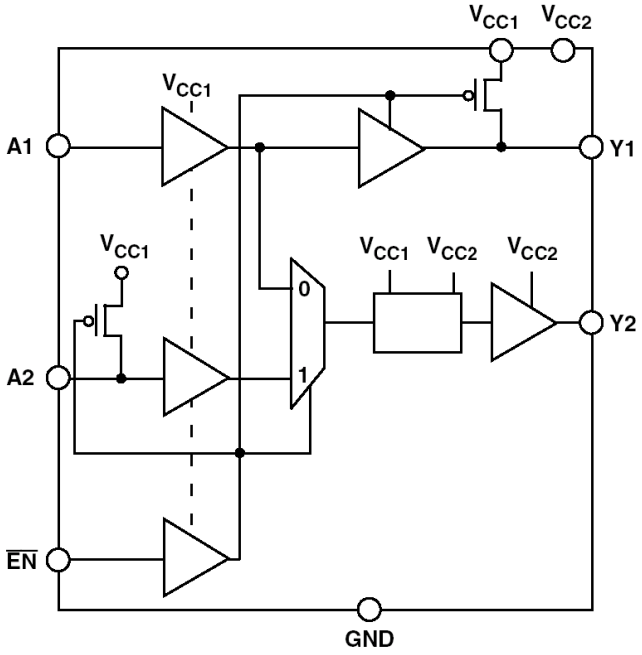


Figure 12: ADG3233 Low Voltage 1.65 V to 3.6 V, Logic Level Translator and Bypass Switch

Figure 13 shows the bypass switch being used in normal mode. In this mode, the signal paths are from A1 to Y1 and A2 to Y2. The device will level translate the signal applied to A1 to a V_{CC1} logic level (this level translation can be either to a higher or lower supply) and route the signal to the Y1 output, which will have standard V_{OL}/V_{OH} levels for V_{CC1} supplies. The signal is then passed through Device 1 and back to the A2 input pin of the bypass switch. The logic level inputs of A2 are with respect to the V_{CC1} supply. The signal will be level translated from V_{CC1} to V_{CC2} and routed to the Y2 output pin of the bypass switch. Y2 output logic levels are with respect to the V_{CC2} supply.

Figure 14 illustrates the device as used in bypass operation. The signal path is now from A1 directly to Y2, thus bypassing Device 1 completely. The signal will be level translated to a V_{CC2} logic level and available on Y2, where it may be applied directly to the input of Device 2. In bypass mode, Y1 is pulled up to V_{CC1}. The three supplies in Figures 13 and 14 may be any combination of supplies, i.e., V_{CC0}, V_{CC1}, and V_{CC2} may be any combination of supplies, for example, 1.8 V, 2.5 V, and 3.3 V.

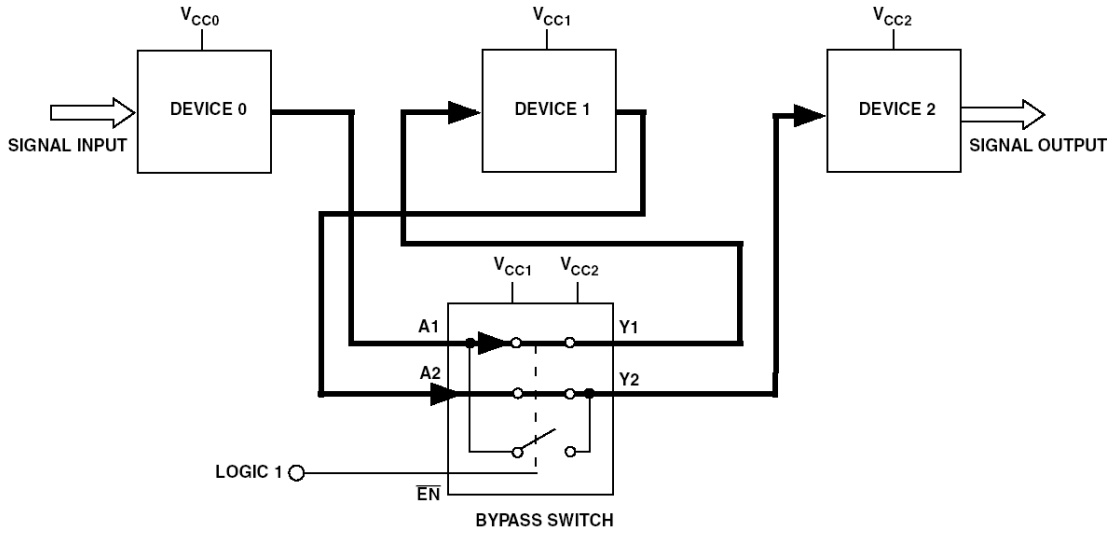


Figure 13: ADG3233 Bypass Switch in Normal Mode

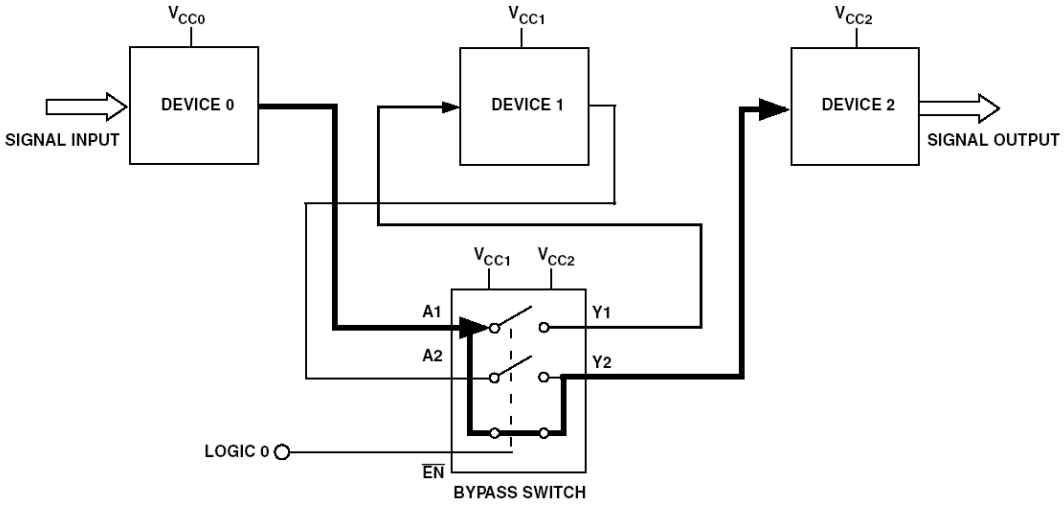


Figure 14: ADG3233 Bypass Switch in Bypass Mode

INTERNALLY CREATED VOLTAGE TOLERANCE / COMPLIANCE

Modern high performance CMOS DSPs and microprocessors typically operate on core voltages between 1 V and 2 V. These low voltages yield optimum speed-power performance. However, the logic levels in the core are not compatible with standard 2.5 V or 3.3 V I/O interfaces. This problem is typically solved as shown in Figure 15, where the logic core operates at a reduced voltage, but the output drivers operate at a standard supply voltage level of 2.5 V or 3.3 V.

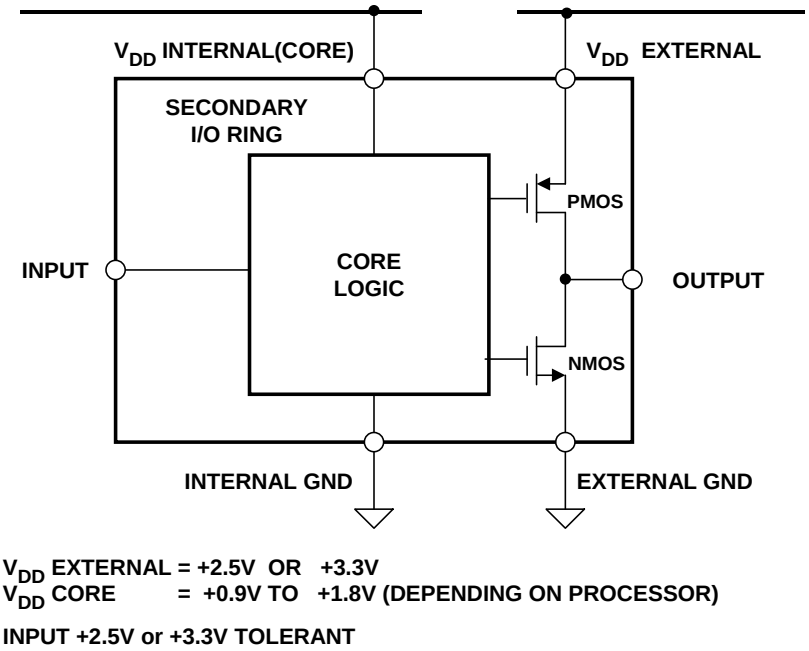


Figure 15: Internal Compliance and Tolerance in a CMOS IC With Secondary I/O Ring

The technique followed by many IC manufacturers is to provide a secondary I/O ring, i.e., the I/O drivers are driven by the 2.5 V or 3.3 V power supply, hence the device is compatible with 2.5 V or 3.3 V logic levels. Note that the inputs must be compliant and tolerant to the I/O supply voltage. There are several issues to consider in a dual-supply logic IC design of this type:

- *Power-Up Sequencing*: If two power supplies are required to give an IC additional tolerance / compliance, what is the power-up sequence? Is it a requirement that the power supplies are switched on simultaneously or can the device only have a voltage supplied on the core or only on the I/O ring? This problem can be easily solved if the core voltage is generated from the I/O supply voltage using a low dropout linear regulator. Sequencing circuits can also be used to solve these issues.

- *Process Support and Electro-Static Discharge (ESD) Protection*: The transistors created in the IC's fabrication process must be able to both withstand and drive high voltages. The high voltage transistors create additional fabrication costs since they require more processing steps to build in high voltage tolerance. Designs with standard transistors require additional circuitry. The I/O drivers must also provide ESD protection for the device. Most current

designs limit the overvoltage to below one diode drop (0.7 V) above the power supply. Protection for larger overvoltage requires more diodes in series.

- *Internal High Voltage Generation*: The PMOS transistors need to be placed in a substrate well which is tied to the highest on-chip voltage to prevent lateral diodes from turning on and drawing excessive current. This high voltage can either be generated on chip using charge pumps or from an external supply. This requirement can make the design complex, since one cannot efficiently use charge pumps to generate higher voltages and also achieve low standby current. In most cases, the voltage is supplied externally.

- *Chip Area*: Die size is a primary factor in reducing costs and increasing yields. Tolerance and compliance circuitry may require either more or larger I/O devices to achieve the desired performance levels.

- *Testing*: Since the core and the I/O can be at different voltages, testing the device for all possible combinations of voltages can be complicated, adding to the total cost of the IC.

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