OSI APP NOTE

Subject: 6502 Clock Circuits #4A

This APP Note superceeds APP Note #4. It contains crucially important information on 6502 clock circuits and high speed operation.

There are several versions of the 6502 available which are not directly compatible with each other! The labeling on the package cap will indicate which unit you have. The format is:

```
   MOS
MCS 6502X
  Y DDDD
```

where X is the speed, Y is the mask revision, and DDDD is the date code.

If X is blank, the chip is a 1MHz guaranteed unit. The chips will typically operate at 1.5MHz. If X is an "A", the chip is a 2MHz guaranteed unit. Through 9-76 date codes, no further speed selection beyond A was made so some "A" chips will run at up to 10MHz! Eventually, "B" (3MHz) and "C" (4MHz) chips will be selected out of the A class of chips.

As of the publication of this APP Note there are two mask versions (Y indicator); blank and C (not to be confused with C speed indication). A blank in the mask indicator specifies that the chip will not execute the "ROR" class of instructions. However, this revision chip will operate with the simple R-C clock in the 400 manual (No OSI software uses ROR instructions). The C mask chips execute the "ROR" class of instructions but will not operate with the simple RC clock of the earlier chips. An external TTL clock should be used such as the one shown in Diagram One. This clock is a variation of the 6800 clock already on the 400 board.

The internal clock was dropped from the current revision chip because it was prone to ringing and produced non-symmetrical Ø1 versus Ø2. For these reasons, we strongly recommend that users of the older chips upgrade to the new clock as they expand their system. The clock circuit is compatible with all 6502 chips.

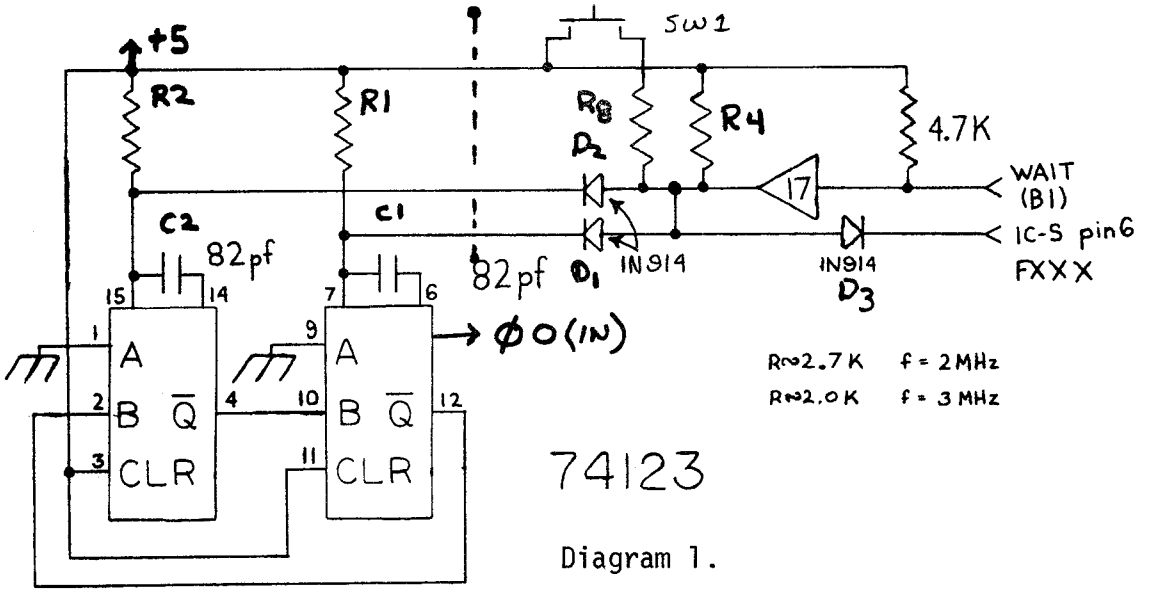

Diagram 1.

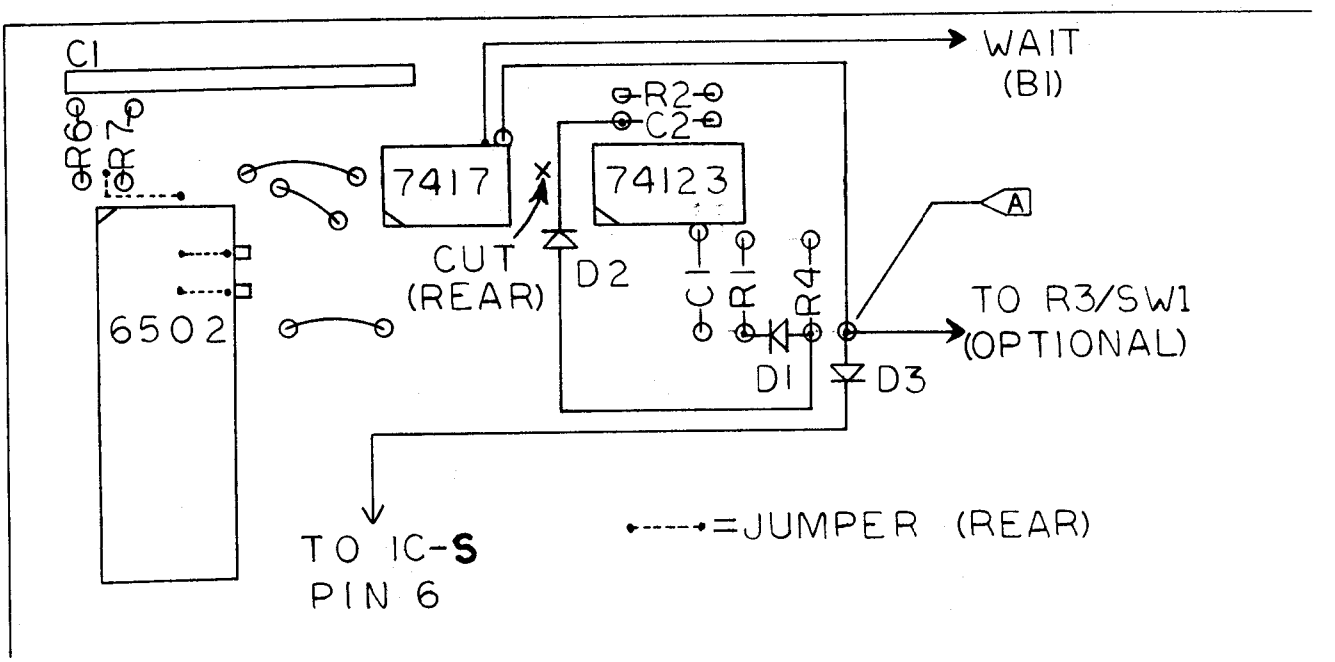

Diagram 2.

Diagram 2 is an exact parts overlay to be used with Diagram 1. To initially implement the circuit, only the components to the left of the dashed line are needed. This produces a single speed clock.

To implement the circuit, use the following directions:

1. Install a 74123 at IC-3. A Texas Instruments or ITT unit is prefered for maximum stability.
2. Cut the foil to pin 13 of the 74123.
3. Install 2 82pf. temperature stable capacitors at C_1 and C_2.
4. If your system does not utilize all of the following: 6502A 3702-1 based monitor, and 350ns. memories (i.e. OSI 414 2MHz system) you should install 22K resistors at R_1 and R_2. This will yield an approximately 1.5usec. clock. If you have a 414 or equivalent, use 10K resistors at R_1 and R_3 which yield an 800ns. clock.
5. Install the two jumpers shown on the front of the board directly to the left of the 7417. (The other jumpers shown are specified in the 400 manual)

Clock Options:

The circuitry to the right of the dashed line in Diagram 1 is for high speed operation. The switch SW1 and R8 optionally provide an ultra fast mode for experimentation.

R_4 normally forward biases D_2 and D_1 providing lower effective resistance at R_2 and R_1 and, consequently, high clock frequency. By bringing the 7417 or D_3 low, diodes D_1 and D_2 are back biased, slowing the clock down. In normal use, R_4 is adjusted to run the processor as fast as the main RAM memory will allow reliably and the wait line and direct diode connections to R_4 are used to stretch the clock for slower devices.

R_8 and SW1 would be used for ultra fast operation for experimental purposes. Table 1 lists typical access times. The guaranteed access times should be used normally and the typical access times for experimental purposes optionally.

Table 1.

Part	Access/Cycle Time Guaranteed	Typical
6502	800/1,000	600/750
6502A	350/500	200/250
C1702A	1,000	600
3702-1	550	400
P2102-6	650	400
P2102AL	350	170
6850	550	400
6820	550	400
6820N-1	250	200
6834	750	500

6502 systems with 650ns. RAMs can be operated at 1MHz reliably with clock stretching on the C1702A PROM Monitor only. This is accomplished by using approximately a 4.7K for R_4 in conjunction with 22Ks on R_1 and R_2. Diode D_3 should go to chip enable on the 1702 (pin 14 of IC-8). 6502A systems with 350ns. RAMs can be operated reliably at 2.0MHz using a 2.7K for R_4 and 22K for R_1 and R_2. All PROMs, ACIAs, etc. will have to actuate the wait line via diodes when addressed.

How Fast Can You Go?

6502As in conjunction with 350ns. memories will operate to about 3MHz. 6502s and 650ns. memories operate to about 1.5MHz.

OSI's memory test program 65U-4 is an excellent diagnostic test for high speed operation. If your system passes the memory test program, all is well.

If you desire to run your system above its specified limits do so with a switch and additional parallel resistor as per Diagram 1 which should only be used for experimental purposes (animation, sound processing, etc. where every nanosecond counts).

Crystal Control Clock

Diagram 3 shows a possible crystal control clock and synchronous divider circuit. With a 4MHz crystal, 2.0 and 1.0 MHz outputs are obtained. The crystal control 4MHz oscillator is present on the 470 board if installed in the system.

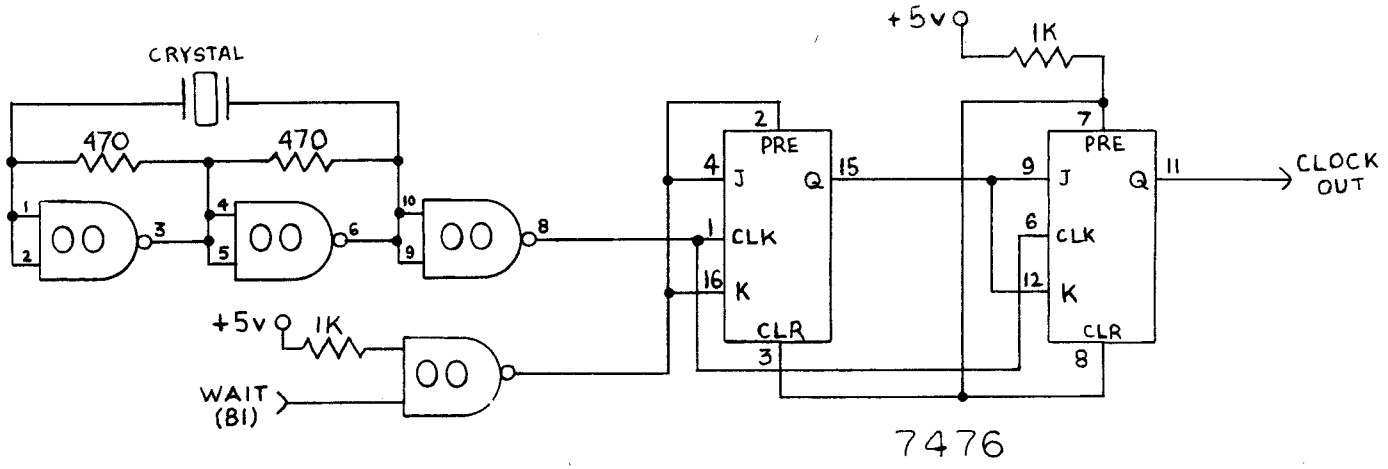
CRYSTAL
470
470
+5v
1K
PRE
J
Q
CLK
K
CLR
CLOCK OUT
+5v
1K
WAIT (B1)
7476

Diagram 3.

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IMPORTANT NOTICE:

IF YOU ARE USING A 6502 MICROPROCESSOR, BE SURE TO READ APP NOTE #4A WHICH IS ENCLOSED BEFORE INSTALLING YOUR CLOCK COMPONENTS.

6502 CHIPS SUPPLIED BY OSI ARE NOW "A" SUFFIX (2 MHZ PARTS) WITH MASK REVISION C. THESE CHIPS HAVE THE ROR INSTRUCTION BUT WILL NOT RUN WITH THE SIMPLE RC CLOCK OF THE EARLIER NON-ROR CHIPS.

OSI SUPPLIED PARTS KITS INCLUDE COMPONENTS FOR THE SINGLE SPEED VERSION OF THE CLOCK SHOWN IN APP NOTE 4A WHICH MUST BE USED WITH THIS PROCESSOR.