How to maintain the CONSUL-580 and the MRD-380

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58-3020

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1. INTRODUCTION

This manual is intended for use by personnel who must perform fault diagnosis and repair of the Consul 580. The reader should be familiar with ADDS publication number 58-3000, How to Use the Consul 580, which presents complete operating instructions and interface information. Before proceeding with the theory of operation, salient terminal features are described below.

1.1 General Description

The Consul 580 is a low cost TTY compatible CRT display terminal. It is designed for users who wish to take advantage of a CRT's silent operation, fast transmission speed and inherent reliability. It is a self-contained desktop unit.

The 580 displays data in format of 24 lines with 80 characters per line - making a total of 1920 characters. Data is displayed as black characters on a white background. Communication with the data processing system or minicomputer takes place in a manner identical to that used by teletypewriters; a character at a time on a conversational basis.

A rack-mountable version of the 580 is available; it is designated the MRD-380 Series. This equipment consists of:

- An electronics package which consists of the terminal electronics (same P.C. cards as the 580) in a chassis suitable for mounting in standard 19" RETMA racks. Vertical panel height is 5-1/4 inches.

- A separate keyboard, in its own housing, which plugs into the 380 electronics package.

- A TV monitor which connects via 75-Ohm coaxial cable to the electronics package.

1.2 Summary of Terminal Features

EIA and Current Loop Interfaces

An EIA RS232C voltage interface and a 20 milliampere current loop interface are standard; both are operational over the full speed range of the terminal - up to 9600 baud.

Five Transmission Speeds

Transmission rates of 110, 300, 1200, 2400 or 9600 baud are selectable by means of a switch on the rear panel of the 580.

Selection of Half and Full Duplex

The operator's FULL DUP switch permits selection of full or half duplex operation.

Automatic Line Feed Selection

A switch labeled AUTO LF allows the operator to inhibit or enable an automatic internal Line Feed after receipt of a Carriage Return code.

Roll Mode Selection

The operator of a 580 can inhibit or enable the upward scrolling of data through use of the ROLL switch. Depressing this switch enables data to scroll upward if the cursor is in the bottom line and a Cursor Down or Line Feed command is received from the keyboard or CPU.

Cursor Control

Cursor controls to position the cursor up, down, forward, backward and home are available. Home is the lower left corner of the screen when the 580 is scrolling data. When scrolling is inhibited, home is the upper left corner of the screen.

Printer Interface

A printer interface allows attachment of any serial EIA printer. The operator can control the flow of data to the printer by using the PRINT ON and PRINT OFF keys on the 580 keyboard.

Audible Alarm

The BEL code causes an audible alarm in the 580 to be activated.

Remote Control

Remote control commands for the 580 are available to perform Carriage Return and Line Feed operations, erase the screen and move the cursor up, down, forward, backward and home. In addition, the CPU can lock and unlock the keyboard, activate the audible alarm and turn the printer interface on and off.

Cursor Addressing

The computer can address the cursor to any given position on the screen. Addressing is provided by two command codes:

a Vertical Address command and a Horizontal Address command. Each of these commands is followed by a character that determines the desired cursor position.

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2. THEORY OF OPERATION

This section presents a block diagram overview of the 580 electronics, followed by a detailed circuit description at the chip level.

Diagrams which should be referenced when reading more than one page of the manual are designed as "fold-out" drawings to aid in following the discussion. An alphabetical Glossary of signal names is presented in Section 3 of this manual for convenience in following circuit descriptions.

Note: Units delivered before January 15, 1974 differ in certain respects from units delivered after that date. Section 10 of this manual contains schematic drawings for both versions of the terminal. In areas where difference exist they are clearly called out in the circuit description. If any doubt exists about which version you have, put the terminal in Half-Duplex mode and press Control-G on the keyboard. If an audible alarm sounds you have the more recent version.

2.1 General Summary

The Consul 580 electronics package is made up of three basic blocks, the Front End, the Memory and Control Logic and the Video Generator. Each block comprises one printed circuit card.

2.1.1 Front End

The Front End block contains the Serial to Parallel Converter, EIA level shifters, TTY current loop converters, keyboard interface, the control decoding logic, the baud rate clock, and the RS232C control logic.

2.1.2 Memory and Control Logic

This block contains the Display Buffer memory, the one line Refresh Buffer memory, cursor generation logic, scroll logic, and the logic necessary to control access to the Display Buffer memory.

2.1.3 Video Generator

The Video Generator contains the master oscillator counters for controlling all video signals, the video amplifier and mixer, sync and blanking generator, Memory timing generator, character generator, Display Buffer address register, and the Address comparison circuitry for memory input.

2.2 Overall Block Diagram Description - (Figure 2.1, page 2-5/6)

The block diagram shows the three major sections divided by dashed lines.

2.2.1 Front End

2.2.1.1 Input Data Path

Input data to the Front End can be either current loop or EIA serial data. The serial data stream is converted to TTL levels and applied to the Serial to Parallel Converter (UAR/T, Universal Asynchronous Receiver/Transmitter) which changes the serial data to parallel data. The parallel data (a character) together with a strobe pulse is presented to the decoding and control logic. If the character is displayable it is presented to the Memory and Control Logic for input to the Display Buffer memory. If the Character is an active control character (Erase, Carriage Return, Cursor Up, etc.) the control logic performs the proper task. If the character is from the sixth or seventh column on the ASCII chart (lower case) it is translated to columns 4 and 5 (upper case.) All other characters and Rubout are ignored by the CRT.

2.2.1.2 Output Data Path

Output data is generated only by the keyboard. When the user strikes a key, the ASCII code together with a strobe is presented in parallel to the output character latch. If the proper conditions exist at the RS232C control logic the character is passed on to the UAR/T with a strobe for parallel to serial conversion. The serialized character is then converted from TTL levels to EIA or current loop signals and passed on to the Modem or CPU.

2.2.1.3 Full/Half Duplex Modes

Full/Half Duplex is controled by a switch above the keyboard. In Full Duplex mode (switch depressed) the serial TTL output goes only to the level converters for output. When the FDX/HDX switch in the Half Duplex position (released) the TTL output data is applied to the serial input of the UAR/T. This causes the character from the keyboard to be treated as an input character from the CPU.

2.2.1.4 RS232C Control Logic

The RS232C Control Logic handles all the necessary control lines to and from the serial data connector. Request to Send is raised when the first character of a message is keyed. As soon as Clear to Send is true (from the Modem or CPU) the latched character is loaded into the UAR/T for transmission. The reverse channel signals SCF and SCA are also controlled by this logic.

2.2.2 Memory and Control Logic

2.2.2.1 Access Control

The Access Control accepts control signals from the Front End and performs the task requested. These tasks include data input, erase functions, and scrolling. In addition there is logic to generate the cursor and logic to handle the updating of the one line Refresh memory.

2.2.2.2 Display Buffer

The Display Buffer memory is composed of MOS shift registers that recirculate their contents at a 1.6 MHZ shift rate. The memory is modular in that it is divided into three sections. Each section has a capacity of 3840 bits or 640 6-bit characters.

2.2.2.3 Refresh Memory

The Refresh Memory has a capacity sufficient to hold 100 6-bit characters out of which only 80 are used for display. This MOS shift register is used to hold one line of characters during the time the Video Generator is generating that particular line of data on the T.V. screen. It is updated from the Display Buffer before the next line is to be displayed.

2.2.3 Video Generator

2.2.3.1 Character Generator

The Character Generator accepts one character at a time from the Refresh memory and then outputs the proper portion of the character to be displayed. The line of characters in the Refresh memory is presented to the Video Generator seven times to complete the display of that data line.

2.2.3.2 Blank and Sync Generators

The Blank and Sync generators mix their signals with the display video to produce the proper signals to frame the data and drive the T.V. monitor.

2.2.3.3 Clock and Timing Chain

The Clock and Timing Chain is used to generate all the timing concerned with the video presentation and the memories.

2.2.3.4 Address Register

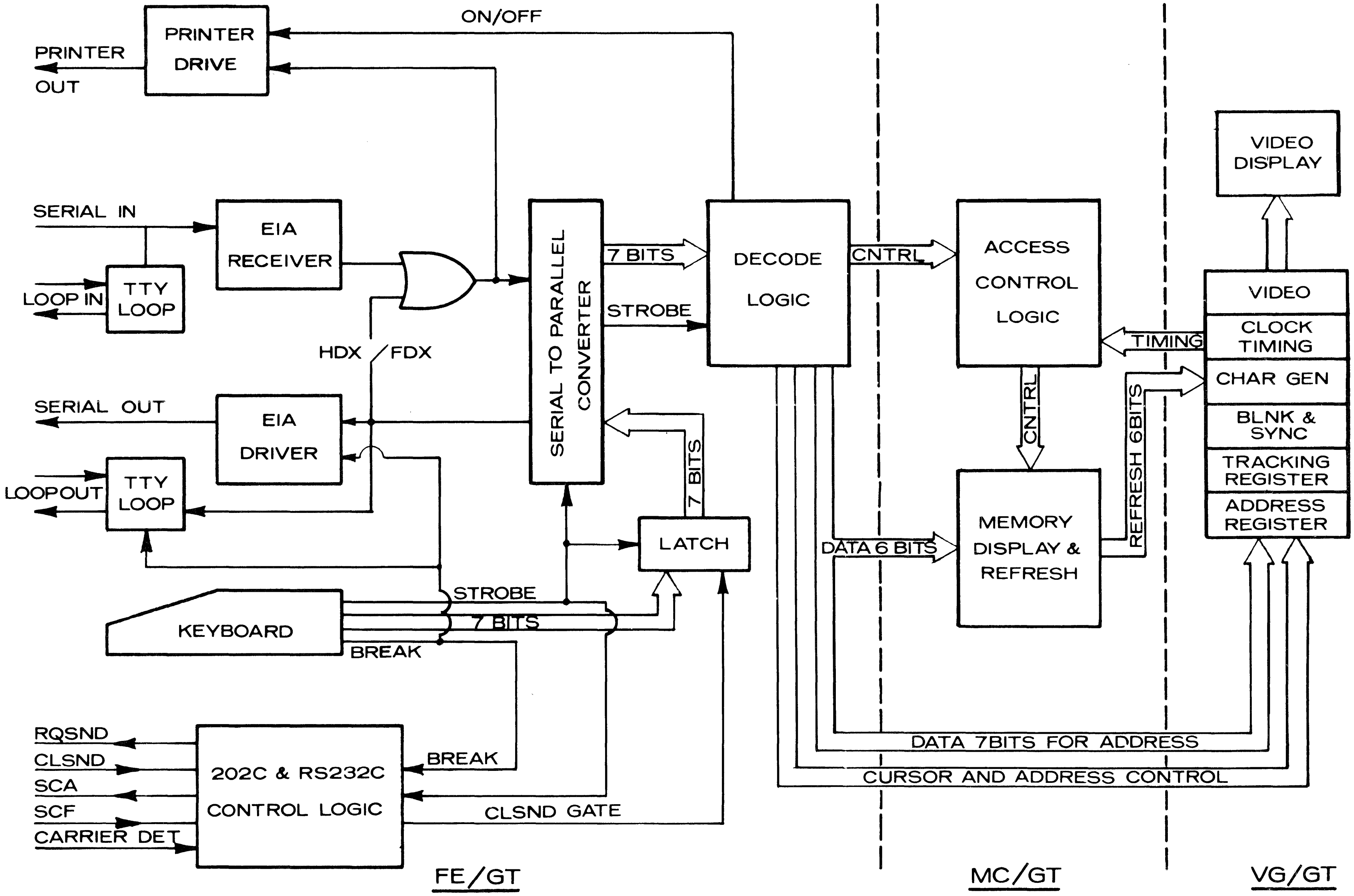
The Address Register contains the address of the next location in which a character may be entered into the Display Buffer.

2.2.3.5 Tracking Register

The Tracking Register counts the shift pulses to the Display Buffer. Its contents at any given time contain the address of the Memory Buffer location that may be accessed.

580 BLOCK DIAGRAM

Fig. 2·1



2.3 Detailed Description - Video Generator

The Video Generator will be discussed first because a large portion of the overall timing and control is generated by this P.C. card.

2.3.1 Video Generator Block Diagram Description (Figure 2.2, page 2-11/12)

2.3.1.1 Clock and Timing Chain

The heart of the Video Generator is the crystal clock and count down timing chain. The clock is a square wave generator with a frequency of 12.528 MHZ. This is the video shift frequency or the rate at which the individual bits of a character are written on the T.V. screen.

The first counter divides this by 8 to a frequency of 1.566 MHZ which is the rate at which complete characters are written on the screen. Timing is derived from this counter for all intra-character clocks and strobes.

The character rate is then divided by 100 to produce the video scan line rate of 15,660 HZ. The signals Horizontal Blank, Horizontal Drive, and Horizontal sync are decoded from this counter.

The next counter divides by 9 to obtain the character line rate of 1740 HZ. Seven of the video scan lines are used to generate the data line and two are used for separation and the cursor mark. The counter outputs are used by the ROM (Read Only Memory) Character Generator to determine which one of the seven horizontal segments of a character should be output to the video.

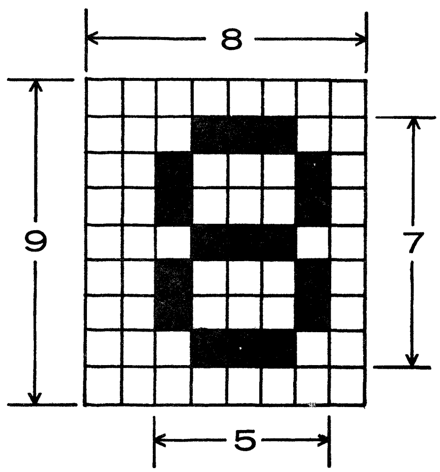
The last counter divides down to the screen refresh rate of 60 HZ (50HZ for overseas models). Signals such as Vertical Blank, Vertical Drive and Memory Select are obtained by decoding this counter.

2.3.1.2 Character Generator

The 580 employs a 5 x 7 dot matrix to generate the 64 displayable characters. Each 5 x 7 character is displayed in an 8 by 9 field. (see Figure 2.3 at top of next page) This gives a three dot horizontal spacing between characters and a two scan line spacing between rows of characters.

CHARACTER MATRIX

Fig.2·3



To generate a character on the screen the Read Only Memory, ROM, must supply seven five-bit words to the video shift register, one for each of the seven scan lines used to display the character. During each scan line at the given character position the video shift register shifts the five bits to the video mixer at the 12.528 MHZ rate. These bits make the video black for ones and white for zeroes, assuming a normal black on white presentation.

The pattern in the ROM is selected by the 6-bit (1 of 64) character latched from the Refresh Buffer memory. This 6-bit word is used as an address to select one of the 64 possible dot patterns. The three inputs S1, S2, and S4 are bits from the scan line counter which select which one of the seven five-bit words is to be output by the ROM.

2.3.1.3 Video Mixer and Amplifier

The character bits from the video shift register are mixed with Horizontal Blank, Vertical Blank, Interline Blank and the cursor mark. The Horizontal and Vertical blank signals always cause the screen to be black. The interline blank causes the screen to be white for black-on-white characters and black for white-on-black characters. The cursor mark always inverts the contrast of the interline blank signal.

The video amplifier takes the mixed signal and drives the internal monitor with a 0 to +5V signal. This same output is also resistively mixed with a composite sync signal to generate a 1V. peak-to-peak composite video signal for external monitors.

2.3.1.4 Display Select Generator

Since the Display Buffer is divided into three modules the video generator must select from one of the three sections to request a new line of characters. The outputs SECT 1 and SECT 2 are used by the Memory and Control card to load the Refresh Buffer memory with the proper line of data. SECT 1 and SECT 2 are low for the top third of the screen. SECT 1 is high for the middle and SECT 2 is high for the bottom. These two signals are obtained from the last counter in the countdown chain which is counting groups of 9 scan lines, or data lines.

2.3.1.5 Internal Video Drive Generator

The internal monitor (Consul 580 only) requires separate signals for Vertical and Horizontal drive. These are TTL levels and are decoded from the timing chain.

2.3.1.6 Memory Clock Generator

All the timing for the memory shift registers is obtained from the Dot Counter. The two phases Ø1 and Ø2 are TTL level 25% duty cycle pulses.

2.3.1.7 Memory Address and Tracking Registers

The Memory Address register is made up of four counters. The first is a decade counter (0 - 9). The second is binary and counts from 0 to 7. These two counters together determine a single line (0 - 79 characters). The third counter counts from 0 to 7 which represents the number of 80-character lines in any one memory module. The last counter is a count of three (0 - 2) which determines which of the three memory modules is to be accessed. All four are synchronous up/down counters. The Address Counter is static and can be changed by the cursor controls or by direct addressing. The contents are automatically updated by an access to memory.

The Tracking Register is made up from three counters which are the same as the first three stages of the Address Register. This keeps track of the position of the circulating Memory Buffer registers. Since the three memory modules are running in parallel only eight lines of eighty characters (one module) have to be tracked.

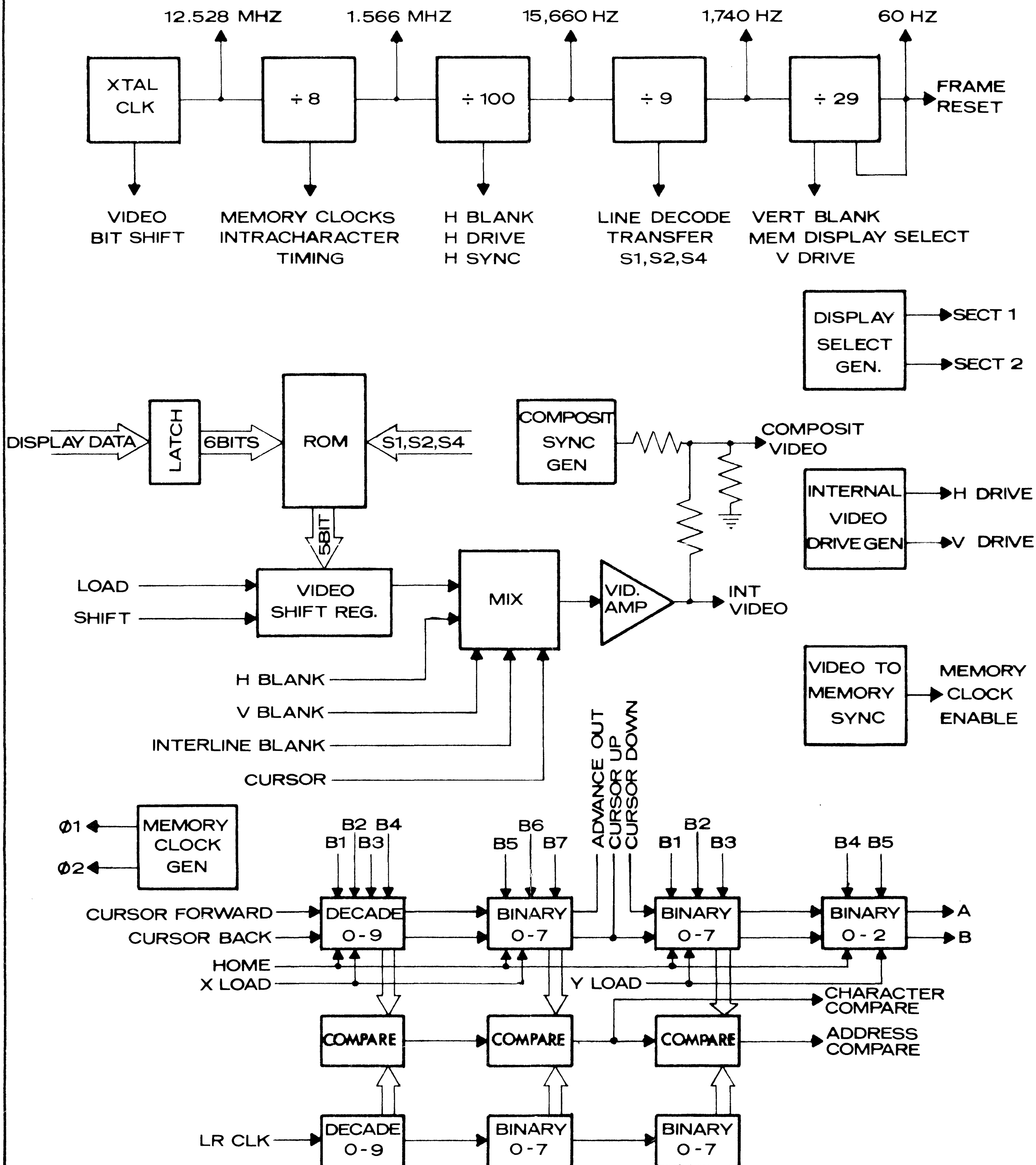
A comparison is made between the Tracking Register and the Address Register. When they have the same value it means that the Memory is at a position such that the character at the location indicated by the Address Register may be accessed. A sub-comparison of only the horizontal location (one of 80 positions) is also made and is used by the Memory and Control board to generate the cursor.

2.3.1.8 Video to Memory Sync Circuit

When the Video Generator finishes a complete scan of the screen the Display Buffer memory is not in sync with the video. The memory sync circuit causes the memory to pause every other scan line until the system is back in sync again.

VIDEO GENERATOR BLOCK DIAGRAM

Fig. 2·2



2.3.2 Circuit Description - Schematic #135-080

2.3.2.1 Clock and Timing Chain

The crystal oscillator is located in the upper left corner of the print. It consists of a common base amplifying stage Q1, driving an emitter follower, Q2, which drives the crystal in the feedback path. The output signal is picked off the collector of Q2 to avoid disturbing the oscillator circuit and drives Q3 in switching mode. The diode, D1, is used to insure a symmetrical load on Q2 and also to protect the base of Q3 from excessive negative voltage. The collector of Q3 drives two Schottky hex inverters (L7,3 and L7,5) in parallel to provide the main clock signal, CLK.

The signal, CLK (12.528 MHZ), drives the first stage of the timing chain K7. K7 is an SN74175N, a quad D-type flip-flop. K7, the Dot Counter, is used as a Johnson or Ring counter. The stages are wired as a shift register with the last stage's complimented output fed to the first stage input. This causes the register to sequentially fill with ones, then zeroes. An entire period takes eight clock pulses. Since only one stage changes state at a time, any state may be decoded with a two-input gate. The three-input nand gate, J6, is used to insure that no illegal state, such as 1010, may exist for more than one period. All intracharacter timing is derived from this counter.

The output of the Dot Counter, D4* (1.566 MHZ or 639 nanoseconds) represents one character time and drives the decade counter chip J7. J7 is an SN 74162 which is a synchronous decade counter. The carry output from J7,15 and the clock, D4* drive the next decade counter H7. These two chips, the Character Counter, perform a divide by 100 which represents one video scan line including Horizontal sync and blank times. The period of this counter is 63.9 microseconds or 15,660 HZ.

The output of H7 is inverted and applied as C80* to the input of F7, another decade counter. This chip is wired such that the output S8 is inverted and fed to the synchronous clear input on pin 1. When S8 goes high, the next clock signal at pin 2 will clear the chip to all zeroes resulting in a divide by 9 function. This is the Scan Line Counter and its outputs S1, S2, S4, and S8 are used for timing within one data line of characters.

Finally, the output S8 drives a binary ripple-through counter consisting of E7, an SN7493N, and C7, an SN7474 wired in toggle mode. This is the Data Line Counter. For 60 HZ devices it counts 29 data lines (261 scan lines) and then is reset to zero. For 50HZ the count is 35 data lines or 315 scan lines. The crystal frequencies 12.528MHZ for 60HZ devices and 12.6MHZ for 50HZ devices were picked to produce a 60HZ or 50HZ refresh rate, while keeping the number of scan lines an integral of 9.

The signal RST1 is the reset signal for the Data Line Counter and is generated by the cross-coupled latch B7,3 and B7,6. The latch is set by the four-input nand gate D7,5. Its output goes low for a count of 29 or 35, setting B7,3 high. The other half of the latch is driven by D4* which has just gone true. One half character later D4* goes false, resetting the latch. Meanwhile, RST1 has reset E7 and RST1* has reset both halves of C7. K7, J7, H7, and F7 returned to zero when E7 and C7 reached the reset count.

2.3.2.2 Horizontal Timing

2.3.2.2.1 Horizontal Blank

The Horizontal Blank signal determines the size of the white page on the screen in the horizontal dimension. One character space is left at each end of the 80-character line to form a border resulting in an 18-character time blank signal. HBLANK (A6,6) is set true when a count of 97 (C80, C10, C4, C2, C1) is reached by B1,8 going false. C10C4G is a combination of C10 and C4 with a Strobe CLK* (see three-input "and" gate E6,6). HBLANK resets at a count of 15, (C80*, C10, C4, C1), resulting in a blank time of 18 characters.

2.3.2.2.2 Horizontal Drive

HDRIVE is used by the internal monitor to develop the horizontal sweep. It begins with HBLANK and ends at character position 31 (C20, C10, C1).

2.3.2.2.3 Horizontal Sync

This signal is needed by an external monitor in order to synchronize tis horizontal oscillator. It is contained within the combined sync circuit (section F-4) and is the output of E6,12. It starts during HDV when C8 returns false (character position 0) and lasts until C8 goes true again (C10 and C20 are low). When C8 goes false again, either C10 or C20 is high keeping E6,12 low. This results in a horizontal sync pulse lasting for 8 character times or 5.1 microseconds.

2.3.2.2.4 Data Gate

DATAGT is a signal lasting for 80 character times or 51 microseconds. This period is the time during which the Display Buffer memory shifts (80 shifts). During the balance of the scan line time (12.8 microseconds) the memory pauses. DATAGT is used to begin the shifting and also to gate one line of data from the Display Buffer to the one line Refresh Buffer.

DATAGT is the output of a cross-coupled latch (Section G-4) B7,11. Since there is a one character delay time through the ROM, DATAGT must start one character time before the first character is displayed on the screen. Since there is a one character boundary, DATAGT may begin when HBLANK ends. Note that B7,13 is driven low by the same signal that resets the HBLANK latch (HBRST*). HBRST* occurs at character position 15. For 80 characters therefore DATAGT must end at character position 95. Note that J6,12 will pulse low at location 95 (C80, C10, C4, C1, CLK*). The input CLK* is used as a strobe to insure no false clocking.

2.3.2.3 Vertical Timing

2.3.2.3.1 Vertical Blank

The vertical blank signal, VBLNK, (Section F-1) is generated by a cross-coupled latch A2,8. This signal determines the top and bottom borders of the white page. To allow for one scan line under the cursor in the bottom line, one scan line is added to the page after the last data line. To keep the page symmetrical, a scan line is also added to the top of the page, allowing two scan lines of white above and below the top and bottom data lines.

For 60HZ devices, VBLNK starts when scan line one, SL1, goes true during data line 28 (L16, L8, L4). VBLNK remains true until scan line 9 (S8 true) of data line 3 (L16*, L2, L1) goes true.

For 50HZ devices, VBLNK begins during data line 32 and ends during data line 7.

2.3.2.3.2 Vertical Drive

VDRIVE (Section E-1) is used by the internal monitor and as part of combined sync by the external monitor to initiate the Vertical flyback. It starts with the reset pulse RST1 and ends when L1 returns true 9 scan lines later.

2.3.2.3.3 Memory Module Selection

Since the three sections of the Display Buffer memory are multiplexed at their outputs, the proper section must be selected for input to the one line Refresh memory. The signals SECT 1 and SECT 2 control this gating and are generated by the flip-flop pair A6 in Section E-4.

VDRIV* is used to set both flip-flops to zero which selects Display Buffer module 1. The gating is done on the Memory and Control board. When the first eight data lines have been displayed, A4,12 pulses low (Data line 11 + Scan line 1) setting A5,9 true. This conditions the Memory and Control card to present the next 8 data lines from the second memory module. After 8 more data lines, A4,8 pulses low (Data line 19 + Scan line 1) resetting A5,9 and setting A5,5 which causes the Memory and Control card to present the last 8 data lines from the third memory module. For 50HZ, these decodes are all increased by 4 Data lines to center the display in the larger number of scan lines.

2.3.2.4 Character Generation and Video Mixing

2.3.2.4.1 Basic Dot Matrix

As mentioned earlier, the 580 uses a 5 X 7 matrix to generate the displayable characters. (See Figure 2.4) The character field is an 8-dot wide by 9-scan line high "window". The character is generated within this field in dot positions 2 through 6 and scan lines 1 through 7. It is evident that the ASCII character information for R and S must be available for at least seven scan lines sequentially in order to generate the two characters or the entire line. Each time a scan line is swept across, a 5-dot portion of the character is generated.

The data line consists of 82 windows, 80 of which are used to display characters. The first and eighty-second windows are always spaces and are used as a margin for the white page. There are 24 such data lines in an entire page for a total of 1920 characters.

2.3.2.4.2 Read Only Memory (ROM)

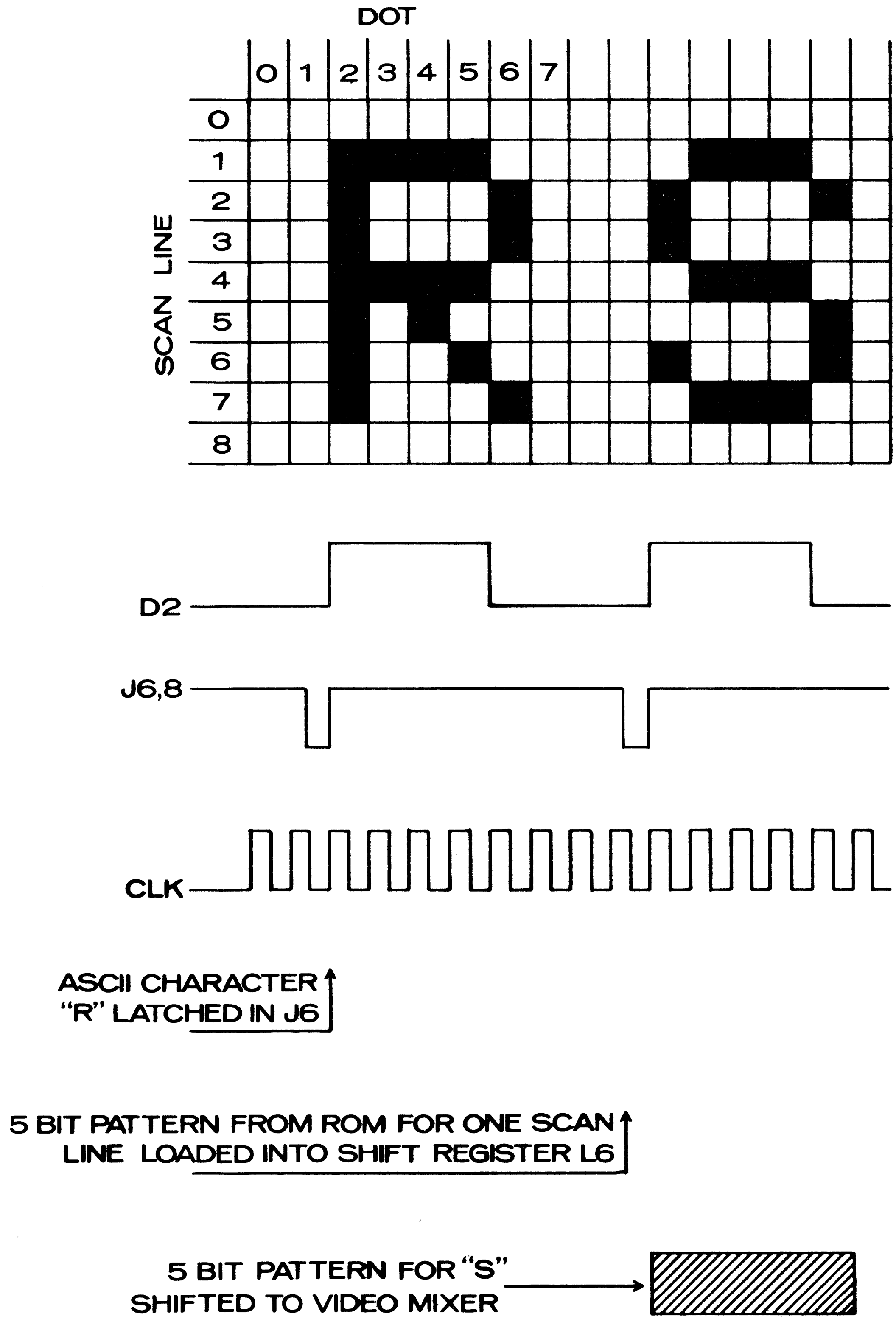
An ROM (Section E-6) is used to store the 64 displayable patterns of 5 X 7 dots. Each pattern is broken down into seven 5-dot words or slices.

Each of the patterns or cells is associated with a 6-bit address (0-63). This address is the same as the ASCII code for the character. For example the ASCII code for an R is 010010-(bit 6 through bit one). This indicates cell #18 which contains the bit pattern for an R. Each five-dot word is addressed by three bits (0-7). The Scan Line Counter bits S1, S2, and S4 are used to address the proper word within a cell. For example, the third 5-bit word of an R pattern is 10001 and is addressed by S1 = 1, S2 = 1 and S4 = 0, which is the state of the Scan Line Counter during the third scan line. The ROM supplies the 5-bit word in parallel at its outputs that corresponds to the selected word in the selected cell.

The ROM used is a static design, which means that the word appears at the output as long as the input address remains stable. Upon an Address change, for instance from the R to the S, that output change is guaranteed to become stable within a maximum of 600 nanoseconds. The character change rate is 639 nanoseconds.

SEQUENTIAL CHARACTER GENERATION

Fig.2·4



2.3.2.4.3 Generation of One 5-bit Character "Slice"

Since the worst case delay through the ROM is 600 nanoseconds, a one character delay is used to allow time for the first character in a line to set up. Using the S as an example in Figure 2.4, note that the ASCII code for S is latched in the holding register J3 by the signal D2; DATAGT became true on the leading edge of D1 allowing D2 to clock the flip-flops. The 5-bit word for the scan line determined by S1, S2, and S4 is stable at the inputs of L6 prior to the load pulse at J6,8. When J6,8 pulses low the 5-bit word is transferred to the shift register L6. The next clock pulse (CLK) on L6,2 shifts the bit pattern by one stage and applies the first bit of the word to the output pin 7. A one in the bit pattern will produce a high level in the shift register and a zero will produce a low level. For the fourth scan line, the 5-bit word would be 01110 which would produce the horizontal middle three dots of the "S". As the first dot of the "S" word is shifted into the output stage the next character to be displayed is latched in the holding register J3.

The output of the shift register is then "AND"-ed with an signal that is true for scan lines 1 through 7 and false for 0 and 8. For a black-on-white presentation the jumper JP1 is installed which enables AND gate E5,5 when the CURSOR signal is low. The character bits are passed by E5 to C1 which inverts the level. B5,1 then inverts again and drives the base of Q4. For a "one" B5,3 is true which turns Q4 on. This causes a low level (0.7V) at the collector and drives the emitter of Q5 to 0 volts which is black on the CRT. A zero bit level causes a +4.3V level at the emitter of Q5 which is white on the CRT. The capacitor C13 is to shape the signal suitably for the monitor's input amplifier. At the same time the internal monitor is receiving a 0 or +4.3 volt signal, the external monitor receives a 0.3V to 1V signal through the resistor network R34, R35, and R36. (CMBSN* is normally high.)

2.3.2.4.4 Blank Mixing

In section F-5 the Vertical Blank, VBLNK, and the Horizontal Blank, HBLNK, are applied through the NOR gate C1,11 and C1,13 to one input of the NAND gate B5,2. When either level is high, B5,2 is blocked causing B5,3 to be high which in turn causes black on the CRT screen regardless of the state of the data signal on B5,1.

2.3.2.4.5 Combined Sync Mixing

The signal CMBSN* in Section E-2 is normally high. At the end of each scan line it pulses low for 5 microseconds to provide a 0V level signal at the external video output (.3V sync, .7V video). At the bottom of the screen, CMBSN* goes low for 9 scan lines to generate the vertical interval step for vertical fly-back. The diodes D9 and D10 are to protect the external output from a monitor failure.

2.3.2.4.6 Miscellaneous

The discrete components around the ROM are needed to supply the proper levels to the device. Input levels must be between ground and +13V. The output drives must be sinked to a negative voltage and caught at +5V by diodes D2-D6 to operate properly with TTL circuits.

In the Video amplifier circuit, the Zener Diode D7 is used to establish a stable +5V switching level independent of TTL switching noise.

The signal CURSOR is generated by the Memory and Control P.C. card. It goes true for 639 nanoseconds in Scan Line 8 under the character whose address is held by the Memory Address Register. This causes an inversion in the background which results in a black underline of white underline depending on the screen background presentation.

2.3.2.5 Address and Tracking Register

The address of the next Display Memory location to be accessed is held by the Memory Address Register consisting of L3, K3, D5 and C6. L3 is an SN74192N, a synchronous up/down decimal counter. This drives K3, an SN74193N, which is a four-stage synchronous up/down binary counter. The two in tandem count from 0 to 79 (only the first 3 stages of K3 are used) or one 80-character line. This portion indicates the horizontal position of the character. The next counter is another SN74193N and is used to indicate which of the eight lines in one memory module contains the character of interest. Finally the two D-type flip-flops of C6 are wired as a synchronous up/down tertiary counter (count of three). This last counter is used to indicate in which of the three memory modules the character location of interest lies.

The Tracking Register is counted by the shift pulse (2) of the Display Memory and indicates which location in any given module is available for access. Its output is stable for one character time and increments at a 1.566 MHZ rate. This register is constructed in the same way as the Address Register in that the first stage is a decade counter, followed by a binary counter. F3 is the decade counter and E3 is a binary counter. Since the three memory modules are shifting together in parallel, only eight lines of 80 characters (one memory module) need be tracked. The last stage of E3 and the two stages of D3 make up the 0-7 counter for the line portion. F3 and the first three stages of E3 made up the character portion.

The three chips F4, E4, and D4 are dual four-bit comparators. These three chips are used to generate a signal that indicates when the memories are at the location held by the Address Counter. This is done be comparing the contents of the character and line portion of the Address Register with the Tracking Register. F4 and E4 compare the character portions and generate a signal named CHCOM, Character Comparison. The output of E4 is gated by COMENB (Comparison Enable) which is true when the memories are not pausing for line end or memory synchronization.

CHCOM is then used with the output of D4 to generate ADDCOM (Address Comparison), the combination of CHCOM and the Line Counter comparison. ADDCOM lasts for 639 nanoseconds and occurs every 510 microseconds except during the memory synchronization time, during which it occurs every 574 microseconds.

The Address Counter is controlled in two basic ways, incremental control and direct addressing. The incremental control is by use of the cursor position keys. The signals generated by the control keys are CURFR* (Cursor Forward Not), CURBK* (Cursor Back Not), CURUP* (Cursor Up Not), ADV* (Advance Not, which is cursor down) and HOME. CURFR* is also automatically pulsed when a memory location is accessed. The signal ADV* is generated from the Cursor Down key or the Line Feed key. It is also automatically generated when the last character in a line is accessed if the terminal is in the Auto Line Feed mode.

The circuitry around L3 is used to insure that an illegal address (greater than 9) can't be stable in the decade register. If stages 2 or 3 are true when stage 4 is true, indicating a number greater than 9, H3,1 will go true. After a delay of 300 nanoseconds (R37 and C19) the reset input L3,14 goes true and resets the counter to all zeroes. The reset level lasts for 300 nanoseconds because of the delay.

The circuitry below K3 is used to generate the line up or down signals necessary when the cursor is made to move from one line to another by forward or backward motion. ADV1, H4,8 pulses low when the first three stages of K3 are true (7) and the up count signal, L3,12 pulses low setting the first three stages back to zero (the fourth stage isn't used). The two nor-gates H3,10 and H3,13 decode the zero state of the counter and the down count pulse to cause the Line Counter D5 to count down one count. In a like manner, the up and down counts for the tertiary counter, C6, are generated at B2,10 and B2,4.

For the count of three function, the flip-flops of C6 are wired in toggle mode. The input clocks are pulsed only when that given stage should change state. For example if C6,9 is true and C6,5 is false then both should change for a down count. The gating structure of D6 with its inputs implements the proper pulses to make C6 operate as an up/down synchronous, tertiary counter. Using the previous example, an up count could cause a positive pulse at B2,10. Since B* is true there will be a clock via D6,1 and 13 to C6,11 which changes C6,9 from a one to a zero. At the same time, since C6,9 was true, A* (C6,8) was false causing B5,6 to be true. This enables the other half of D6 (pins 4 and 5) and causes a clock at C6,3 changing C6,5 from a zero to a one. Note that if a down count occurred, B2,4 would pulse true and only D6,10 is enabled therefore affecting only C6,5.

The nand gate C4,11 is used to insure that the illegal state of A = B = 1 is not stable. If A and B were both true, C4,11 would go low causing a reset at C6,1 lasting for 300 nanoseconds. The second control mode for the Address Register is by direct addressing. For a horizontal address input XLOAD* pulses low and the registers L3 and K3 are loaded with an address determined by the levels of B1 through B7. The three most significant bits B5-B7 select which group of 10 locations (0-9, 10-19----70-79) will be addressed. Bits 1 - 4 select which one of the locations within a group is addressed (0 - 9). The vertical address is input when YLOAD* pulses low. B1 - B3 then indicate which line in a group of 8 is addressed. B4 and B5 indicate which group of 8 or which memory module is addressed.

The signal LSTLNE (Last Line) is true when C6,5 (B) is high, indicating the third memory module, and B1,12 is false indicating a count of 7 in D5. This signal, when true, is used to determine that the memories should scroll data up for a line advance in the scroll mode.

2.3.2.6 Memory to Video Synchronization

In order to explain why synchronization is necessary a discussion of the method used to transfer data from the Display Memory to the one-line Refresh Memory will be given.

As mentioned before, the Display Buffer Memory is divided into three modules of 640 characters each (8 lines of 80). These modules are shifting together with their inputs and outputs multiplexed for access and display. At the top of the white page the first memory module must be ready to transfer the first line of 80 characters to the one line Refresh Memory. This indexes the memory by one line of eighty characters. During the next 8 scan lines the Display Memory shifts for 8 more lines. It is then back to the same relative position as when it completed the transfer of the first line (line 0) to the Refresh. The first line was transferred when the Scan Line Counter F7 was at a count of 8. (The characters are generated in lines one through seven.) After the bottom scan of the characters the Display Memory is ready to shift the next line of characters (line 1) to the Refresh Memory. This process continues until all eight lines have been transferred. Now the Display switches to the second memory for 8 more lines of characters and then to the third module for the bottom eight lines.

Referring to Figure 2.5, the last line transfers to the Refresh Memory during scan line 8 of data line #26. The memories continue to shift as if they were loading data for two more data lines. At the end of these two data lines the video begins the vertical flyback (RST1 pulses at the end of Data Line 28). When the Video Generator is ready to display the first line on the screen, line 0 of memory module 1 must be ready to transfer to the Refresh Memory. In order to achieve this the Display memories must be in synchronism with the Scan Line Counter. That is. line 0 in the Display Memory must shift through the output during scan line 0, memory line 1 with scan line 1, etc., in order for memory line 0 to be ready to shift into the Refresh Memory during scan line 8.

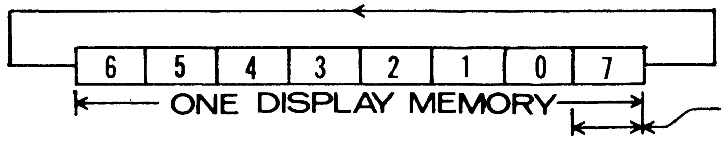
When RST1 pulses, the synchronization circuit in sections D1,2 and 3 begins to lock the memory to the Video Generator. This is done by causing the memories to pause every other scan line until memory line 0 is shifting during scan line zero. The memories are always shifting in groups of 80 shifts in sync with the Video scan line so only the line portion must be brought back into lock.

When the Scan Line Counter outputs S1, S2 and S4 and the Tracking Register outputs TR1, TR2 and TR4 are the same, the memory is in sync with the video. By not allowing the memories to shift during scan line 8, the memories will remain in sync until the first line is needed, at which time the memories will shift during scan line 8 again.

Referring to the schematic drawing, the signal RST1* pulses low at the vertical flyback time setting the flip-flop B4,9 true. One effect of this is to enable NAND gate A2,2 allowing S8 when true to go high; which on the Memory and Control board blocks the clocks that cause the Display memories to shift. Data Gate, DATAGT, goes true at the start of the 80 character shift group and sets B4,5 true allowing A2,6 to go low. During synchronization NAND gate B1,3 is enabled because B4,9 is true. The comparator F6 causes inverter C3,12 to be true when S1, S2 and S4 are not the same as TR1, TR2 and TR4. This causes B1,6 to go

MEMORY SYNCHRONIZATION

Fig. 2·5



DISPLAY MEMORY POSITION AT START OF SCAN LINE 8 IN DATA LINE 26

ONE LINE OF 80 CHARACTERS

MEMORY POSITION AT BEGINNING OF SCAN LINE								SCAN LINE	DATA LINE	
7	6	5	4	3	2	1	0	0		
0	7	6	5	4	3	2	1	1		
1	0	7	6	5	4	3	2	2		
2	1	0	7	6	5	4	3	3		
3	2	1	0	7	6	5	4	4	27	LAST DATA LINE DISPLAY
4	3	2	1	0	7	6	5	5		
5	4	3	2	1	0	7	6	6		
6	5	4	3	2	1	0	7	7		
7	6	5	4	3	2	1	0	8		
0	7	6	5	4	3	2	1	0		← VERTICAL BLANK BEGINS
1	0	7	6	5	4	3	2	1		
2	1	0	7	6	5	4	3	2		
3	2	1	0	7	6	5	4	3		
4	3	2	1	0	7	6	5	4	28	
5	4	3	2	1	0	7	6	5		
6	5	4	3	2	1	0	7	6		
7	6	5	4	3	2	1	0	7		
0	7	6	5	4	3	2	1	8		← RST1 PULSES LOW
1	0	7	6	5	4	3	2	0		
2	1	0	7	6	5	4	3	1		← PAUSE IN SHIFTING
2	1	0	7	6	5	4	3	2		
3	2	1	0	7	6	5	4	3		← PAUSE IN SHIFTING
3	2	1	0	7	6	5	4	4	0	← MEMORIES IN SYN
4	3	2	1	0	7	6	5	5		
5	4	3	2	1	0	7	6	6		
6	5	4	3	2	1	0	7	7		
7	6	5	4	3	2	1	0	8		← PAUSE IN SHIFTING
7	6	5	4	3	2	1	0	0	1	
0	7	6	5	4	3	2	1	1		PAUSE DURING SCAN LINE 8 OF DATA LINES 1&2
1	0	7	6	5	4					
2	1	0	7							
BALANCE OF 1, 2 AND START OF 3							6	6		
				2	1	0	7	7	3	← VERT BLNK END
		5	4	3	2	1	0	8		← FIRST LINE OF DISPLAY SHIFTED INTO REFRESH
0	7	6	5	4	3	2	1	0		
1	0	7	6	5	4	3	2	1		
2	1	0	7	6	5	4	3	2		
3	2	1	0	7	6	5	4	3		
4	3	2	1	0	7	6	5	4	4	
5	4	3	2	1	0	7	6	5		
6	5	4	3	2	1	0	7	6		
7	6	5	4	5	2	1	0	7		
0	7	6	5	6	5	2	1	8		← SECOND LINE LOADED

low when S1 is true. The result is that the memory clocks are disabled during the time S1 is true unitl a true comparison is achieved. It takes two pauses to reach sync because the memories were out of sync by 2 lines when RST1* pulsed low. When synchronization occurs, F6 causes C3,12 to be low which disables B1,6 allowing A2,5 to go true every scan line for 80 shifts. From this point on the memories pause only during scan line 8 to maintain sync. Vertical Blank goes true at the start of scan line 8 in Data Line 3. This transition is used to set B4,9 back to zero allowing the Display memories to shift during scan line 8.

2.4 Detailed Description - Memory and Control

2.4.1 Memory and Control Block Diagram Description (Figure 2.6, pages 2-31/32)

2.4.1.1 Display Memory and Refresh Memory

The Display Memory stores the 1920 characters displayed on the CRT screen. Each character position requires 6 bits because the displayable character set consists of 64 different characters. The memory is a mix of MOS static shift registers and MOS dynamic shift registers. These registers are arranged in three modules of 640 characters each, with 6 bits for each character. The memories shift at the Video character rate of 1.6 MHZ. One module has six 640-bit shift registers running in parallel such that a new 6-bit character appears at the module output every 639 nanoseconds. The outputs from each module are returned to the inputs so that the data renews itself in the memory constantly.

In the block diagram, Data 1 is the 6-bit output of memory module 1 and is returned to the input via the input multiplexer. In order to enter data, the recirculation path of Data 1 is broken for one shift period and new data (INPUT DATA) is gated to the memory input by the input multiplexer and shifted into the memory instead. After the new data has been shifted in, the recirculation path is again closed and the new data remains in memory.

The three memory modules also shift together such that three characters are shifted at a time, one in each module. When data is entered, the input multiplexer breaks the proper recirculation path. The Display Memory clocks are gated in 80-pulse bursts and stopped for 20 character times every scan line such that it takes 8 scan lines to shift 640 times, a complete cycle.

In order for the Video Generator to display a line of characters it needs the 80 character codes for that line at least 7 times for 7 sequential scan lines. The Refresh memory is used to store the one line of 80 characters for 9 scan lines (7 of which are actually used to generate characters). The Refresh memory consists of six 100-bit shift registers in parallel which shift at the Video character rate of 1.6 MHZ. The display select and recirculation control logic transfers one line of 80 characters from the proper Display Memory module to the Refresh memory once every nine scan lines. It does this by breaking the recirculation path of the Refresh memory for one scan line and allowing the data from one of the Display memories to be shifted in. Only the 80 positions filled by the one line of characters are used by the Video Generator. The clocks to the Refresh memory are not gated since the memory is the same length as one scan line (100 characters).

2.4.1.2 Access Logic

The access logic controls the input of a character to the Display Memory. The inputs A and B select which module is to be accessed. When the memories are in such a position that the character to be replaced is ready to be shifted from the output back to the input (Address Comparison true), the proper load pulse (LOAD 1, 2 or 3) pulses true. The load pulse causes the recirculation path to break for the one character time necessary to shift in the new data. The signal CLRG is used to force space code into the inputs of the memory modules for an Erase function.

[For units delivered before January 15, 1974, note that the force signals are CLEAR 1, 2, and 3. Also note that space code was forced for Carriage Return as well as for the Erase function.]

2.4.1.3 Scroll Logic

This section controls the scrolling of data up the screen. When the Memory Address register indicates the cursor is in the the last line (LSTNE true) and the Video Generator indicates that the Address has just gone through the last position on a line (ADV1* pulses low), the circuit causes a scroll. At the same time the signal normally causing the Memory Address to change by a line (ADV*) is not allowed to pulse. Scrolling is accomplished by making the three memories into one memory of 1920 characters for 80 shifts. This is done by gating the output of memory #2 to the input of memory #1, and memory #3 to memory #2. Space code is input to memory #3. Thus all data is shifted up by 80 characters, or one line.

This circuit also blocks the ADV* signal normally generated by a Carriage Return when the terminal is not in Auto Line Feed mode. The ADV* then pulses for only cursor down or Line Feed (same code).

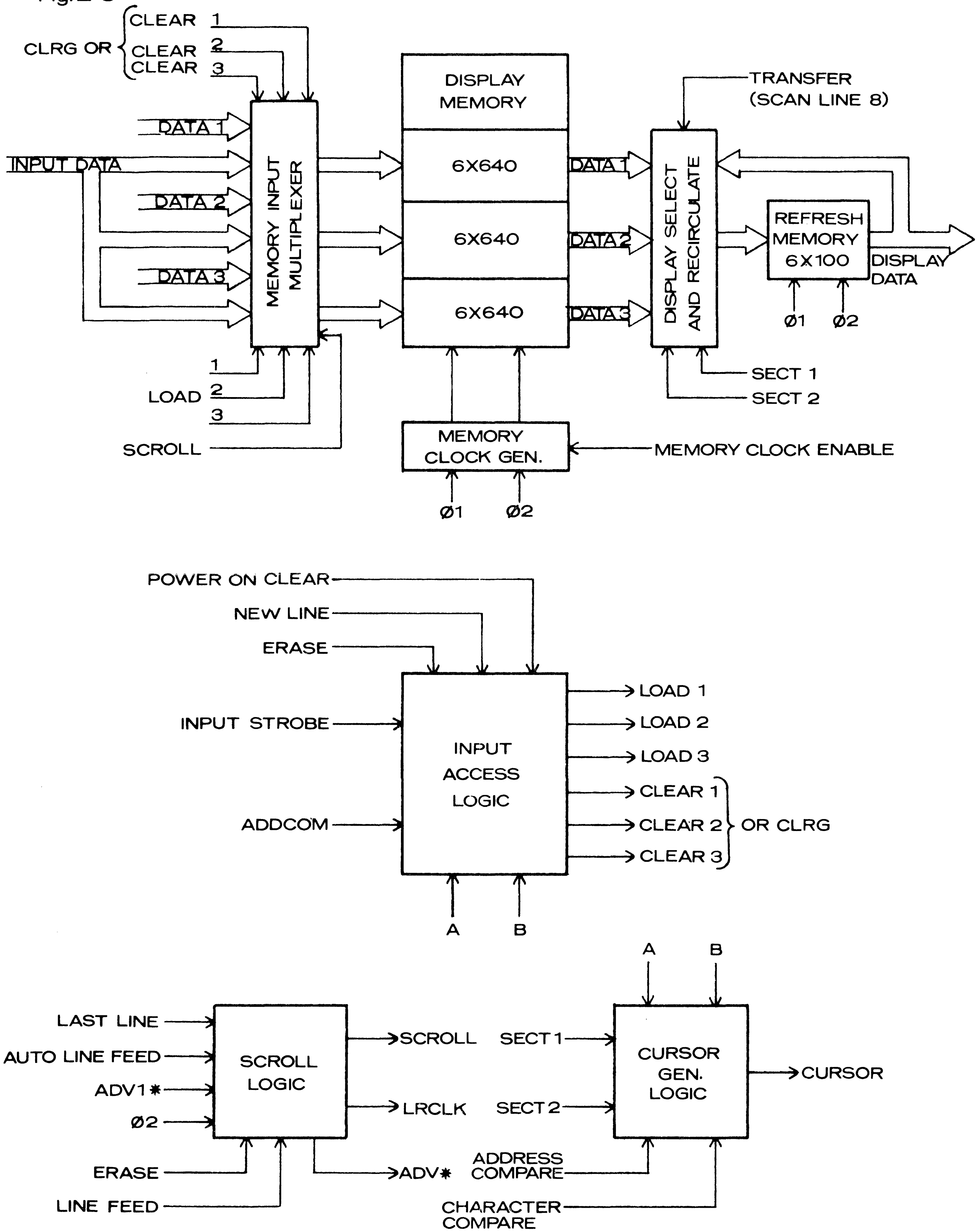
2.4.1.4 Cursor Generation

The cursor is generated as follows:
When Address Comparison is true during Scan Line 8 it means that the character of interest is being loaded into the Refresh memory. The next time Scan Line 8 goes true the cursor must be generated in order to place it under this character. When the signal Character Comparison goes true during the next Scan Line 8 the cursor signal is generated after being delayed by one character time. The delay is necessary because of the one character delay through the ROM character generator. On the Video Generator card the CURSOR pulse inverts the background level causing the underline mark.

(Intentionally left blank)

MEMORY & CONTROL BLOCK DIAGRAM

Fig. 2·6



2.4.2 Circuit Description - Refer to Schematic #135-081

2.4.2.1 Display and Refresh Memory

The Display Memory is a group of shift registers running in parallel and recirculating their contents from output back to input. A single bit is composed of a 128-bit static register in series with a 512-bit dynamic register to make a single shift register 640 bits long. Six such register combinations make up one 6 x 640 bit memory module. Three memory modules make up the entire Display Memory of 1920 6-bit characters.

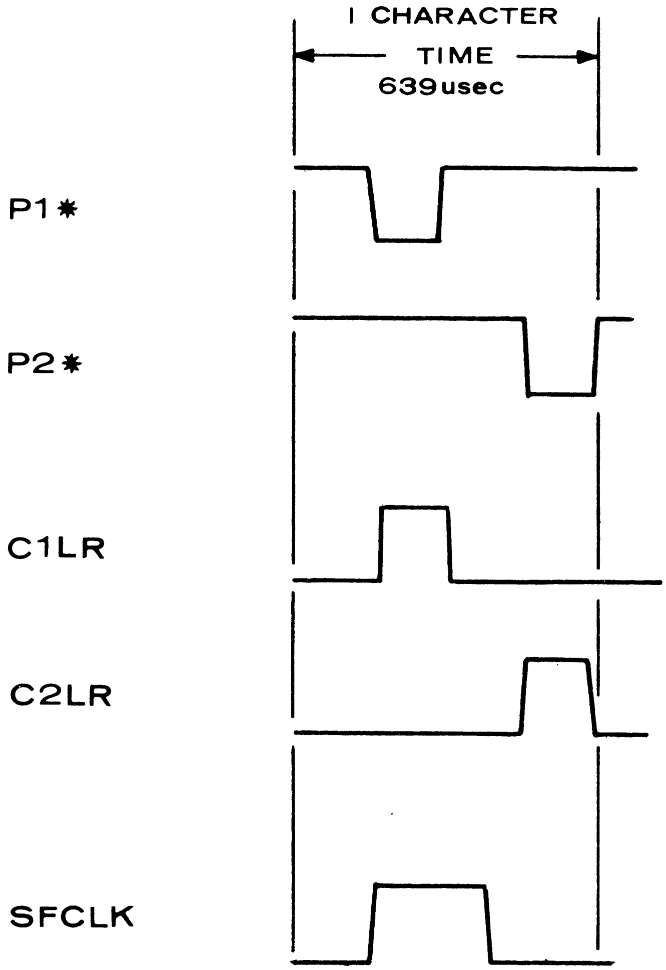
The static registers are quad 128-bit devices, MM5055. The dynamic registers are dual 512-bit devices, MM5017. Memory module #1 consists of K6, 1/2 of H6, K5, L5, and H5. In order to show the recirculation path, Bit 1 of module #1 will be used. The data path around the memory is as follows:
The output is K5 pin 5 buffered by the AND gate L6,3 and is named M1. M1 is positive for 1 and zero for a 0. M1 is applied to the input of the dual four-bit multiplexer L7,13. Normally this input is passed on to the output L7,9. L7,9 is tied to the input of the static register K6,2 whose output K6,14 drives the input of the dynamic register K5,3 completing the recirculation path.

The Refresh memory is made up from three dual 100-bit dynamic shift registers D3, E3, and F3. Referring to Figure 2.7 on the next page, note P1* and P2*. These two pulses occurring during one character period are used to generate the clocks to shift the Refresh register C1RR and C2RR. D2 is a dual MOS clock driver which outputs the +5 volt to -12 volt clocks C1RR and C2RR. These clocks are not gated because the length of the register equals the number of character positions in a scan line. The data in the Refresh memory is recirculated by the two quad 2-input multiplexers H4 and F4 which normally pass the buffered outputs B1V-B6V to the inputs of the registers. S8 is true during the ninth scan line and gates the data from the Display Memory to the input of the Refresh memory to update its contents for the generation of the next character line.

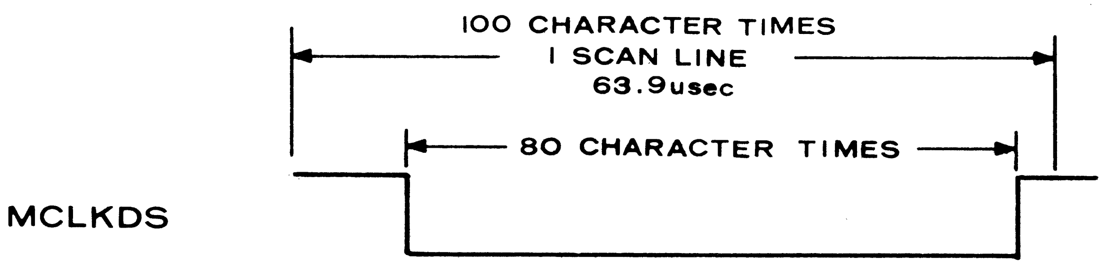
The three dual four-line-to-one-line multiplexers L4, K4 and J4 are used to select which Display Memory module will load the Refresh memory; Module 1 when SECT1 and SECT2 are low, Module 2 for SECT1

Fig. 2·7

TIMING WITHIN ONE CHARACTER



MEMORY SHIFT TIMING FOR ONE SCAN LINE



= 1 and SECT2 = 0, Module 3 when SECT1 = 0 and SECT2 = 1.

The clocks for the dynamic portion of the memory are PH1 and PH2. These are generated from P1* and P2* gated with Memory Clock Disable, MCLKDS, which is low for 80 character times. The transistors are necessary to supply the current for changing the memory clock inputs. The static memory clock is generated from C1LR, (C8,10) by the one-shot J8 is approximately 200 nanoseconds long, SFCLK.

2.4.2.2 Access Logic

2.4.2.2.1 Access For Standard Displayable Characters

When an input to the Display Memory is to be made the signal ACCESS in section F8 pulses true. This sets the flip-flop A8,9 true enabling AND gate C4,5 and resetting flip-flop A8,6 true. When ADDCOM is true, indicating that the Display Memory is in the correct position for input, the D input of flip-flop D4,2 is enabled. The clock input to D4 is the inverse of P1* and sets the flip-flop true at the leading edge of the memory clock C1LR (same time). This releases the clamp on the reset input to D4,13 and causes LOAD* to go low. LOAD* strobes the Dual 1-line-to-4-line data selector (F8), causing LOAD1*, LOAD2* or LOAD3* to go low depending on which memory module is selected by A and B. This load pulse, assume LOAD1*, breaks the recirculation path for the memory module and allows the data B1-B7 (B6 not used) to be entered on the trailing edge of C1LR (Memory Input Clock).

Back in the access logic, note that D4,5 also enables NAND gate B3,4. When C2LR pulses (Memory Output Clock) the signal CURCK* pulses, advancing the cursor one position. At the same time D4,11 is clocked on the trailing edge of C2LR and sets D4,8 false which resets D4,5 low completing the input of one character. As soon as D4,5 returns false it resets D4,8 removing the reset signal on D4,1. When LOAD* pulsed low the input flip-flop A8,9 returned low blocking the next P1* from setting D4,5 true again.

2.4.2.2.2 Access For CR or FF (for units delivered after January 15, 1974)

For a Carriage Return or Erase function the access is handled somewhat differently. For Carriage Return the signal CR will be true. This causes NOR gate C8,1 to be low enabling AND gate B8,1. When ACS goes true (flip-flop A8,9 goes true upon the ACCESS signal generated by the CR input code) the Q output of flip-flop A6,5 goes true. When D4,5 goes true for the first ADDCOM, NAND gate B3,3 goes low clamping D4,5 in the set state. After the first access D4,8 goes low holding the Reset input D4,1 low but since the Preset, pin 4 is also low, output pin 5 of D4 remains high.

If the input code is FF (Erase), the signal CLRG from K8,10 and 13,section G7 is true since CR and CLR* are both low. This breaks the recirculation path of all three memory modules, and zeroes, representing space code, are loaded as long as CLR* is held low. The flip-flop A8,6 goes false when LOAD3* returns true after the third memory module is cleared and then goes true again when LOAD3* goes low and high a second time which clocks the flip-flop A6,5 back false. The reason for two passes through the memory is to insure the entire screen is erased because the cursor is not returned home by the FF operation before it starts.

If the input code is CR (Carriage Return), CLRG is held low preventing any memory module from erasing any data. The LOAD 1, 2, 3* signals are inhibited by CLRFF, F8,1 section B3. CLRFF is the inverse of CR. The Preset clamp on D4,4 is released when A6,5 is returned false. The clock input to A6,3 is driven by ADV1,the inverse of ASV1*, which pulses when the cursor has crossed a line boundary. Since the D input is grounded, the trailing edge of ADV will clock the output back to zero completing the CR function. Keep in mind that the flip-flop A8,6 is true because it was reset with first access and doesn't interfere with the ADV pulse clock.

The signal READY is not used elsewhere in the 580. It is included for possible future use. The READY input to A8,12 is to insure that a second input can't be initiated if the ACCESS logic is busy.

2.4.2.2.3 Access For CR or FF (for units delivered before January 15, 1974)

On earlier units the CR and FF functions were handled as described below.

Consider the Carriage Return function. For Carriage Return the signal CR will be true. This causes NOR gate C8,1 to be low enabling AND gate B8,1. When ACS goes true (flip-flop A8,9 goes true upon the ACCESS signal generated by the CR input code) the Q output of flip-flop A6,5 goes true. When D4,5 goes true for the first ADDCOM, NAND gate B3,3 goes low clamping D4,5 in the set state. After the first access, D4,8 goes low holding the Reset input D4,1 low but since the Preset, pin 4 is also low, output pin 5 of D4 remains high. In the upper left corner, note that if one of the LOAD* signals is low and CR is high, one of the CLR1, 2 or 3 signals will go true. This happens because the output of the EXC-OR gate L8,11 is false when CR is true enabling the NOR gates. When for instance LOAD1* goes low the output of NOR gate K8,1 goes true. Since K8,13 is low (CR is true) CLR1 goes true. This breaks the recirculation path of memory module 1 and instead of loading B1-B7, zeroes are loaded, resulting from the clear input on L7, K7 and J7 (representing space code), as long as the load pulse LOAD1* stays low. The load will continue until the flip-flop A6,5 is returned false releasing the Preset clamp on D4,4. The clock input to A6,3 is driven by ADV1,the inverse of ADV1*, which pulses when the cursor has crossed a line boundary. Since the D input is grounded, the trailing edge of ADV will clock the output back to zero completing the CR function. Keep in mind that the flip-flop A8,6 is true because it was reset with first access and doesn't interfere with the ADV pulse clock.

If the input code is FF (Erase) the same thing happens as with a CR but the flip-flop A6,5 doesn't get clocked off by ADV because CR is low. Instead, the flip-flop A8,6 goes false when LOAD3* goes low and high a second time which clocks the flip-flop A6,5 back false. The reason for two passes through the memory is to insure the entire screen is erased because the cursor is not returned home by the FF operation before it starts.

[The signal READY is not used elsewhere in the 580. It is included for possible future use.

The READY input to A8,12 is to insure a second input can't be initiated if the ACCESS logic is busy.]

The signals CLR1, 2 and 3 are all forced true when a FF is done because CR is low disabling NOR gates K8, 1, 4 and 10. When CLR* goes low K8,13 goes true and all the clears go true.

2.4.2.3 Scroll Logic

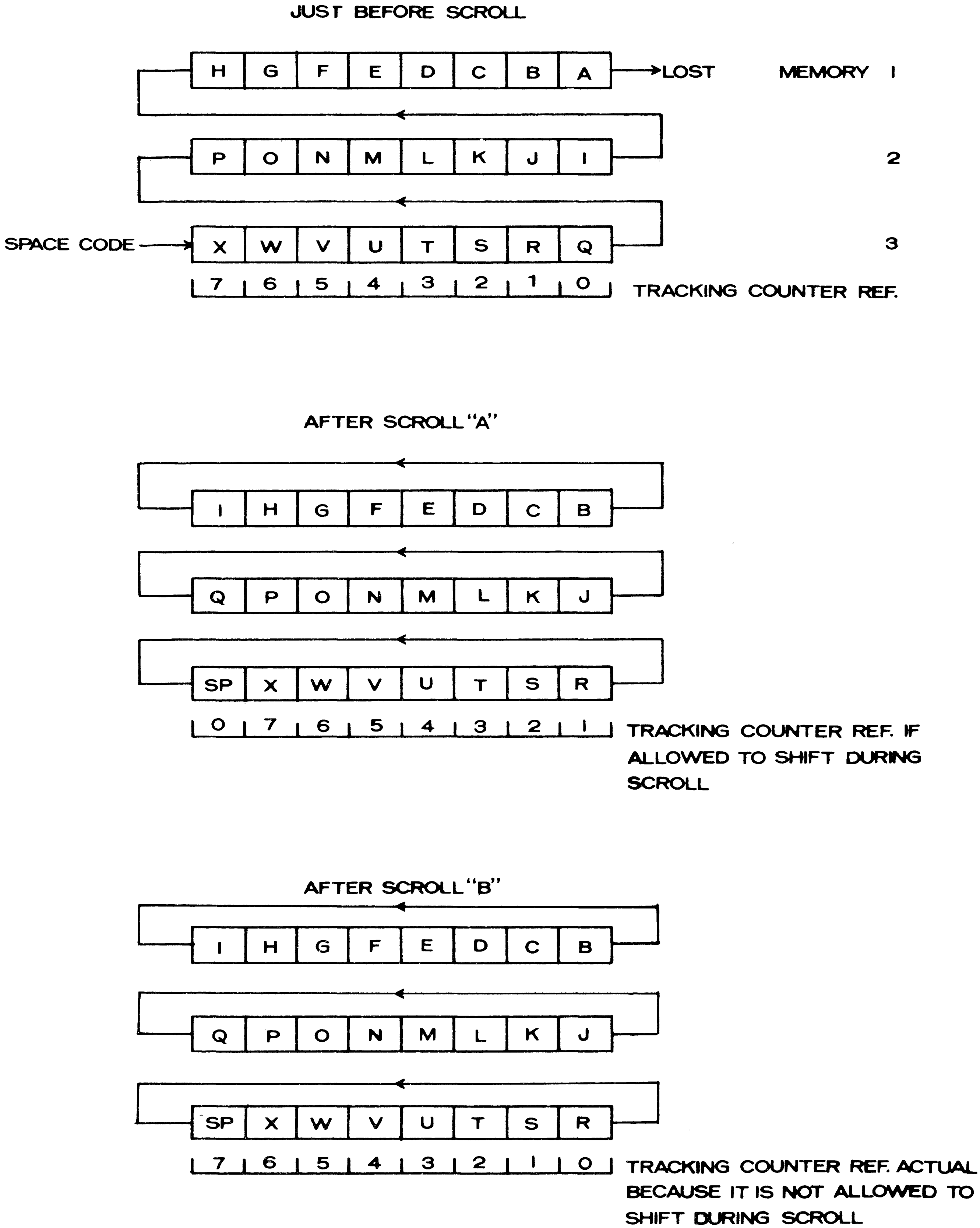
The Scroll circuitry handles two functions, the scrolling of data up the screen and the gating of ADV* which is the signal from the character portion of the Memory Address register which indicates that the cursor has gone from character position 79 to 0 (crossed the end of a line.) If the terminal is in Auto Line Feed, then B3,10 is true which allows ADV1* to pass on through inverted to the input of NAND gate B4,9. If the terminal is in non-ROLL mode or the cursor is not in the bottom line the other input B4,10 will be enabled allowing ADV1* to pass as ADV*. However, if the terminal is not in Auto Line Feed, then ATOLFG is low blocking ADV1* at B3,10. Now, in order for ADV* to pulse, a Line Feed code or Cursor Down (same code) must be entered which causes a positive pulse at inverter A2,11 which generates an ADV* pulse advancing the cursor down one line.

In order to understand what occurs when the Memories scroll refer to Figure 2.8. At the top the three memory modules are shown with the output of #3 attached to the input of #2, and the output of #2 attached to the input of #1. The input of #3 is forced to space code while the output of #1 is lost. This occurs when SCROL* into the dual 4 line-to-1 line multiplexers B7, C7, D7, E7, F7, H7, J7, and K7 goes low. When SCROL* is low the memories are attached together as one 1920 character shift register.

Returning to Figure 2.8, the registers are shifted for 80 counts in the long configuration. After 80 shifts the signal SCROL* returns true and the memories are returned to the normal configuration as shown in the middle of Figure 2.8. Note that after the scroll, the 80 spaces in memory #3 are in what would be the position of line 0 or the top line of the group of 8 instead of the bottom

RELATIVE MEMORY POSITIONS DURING & AFTER SCROLLING

Fig. 2·8



line where they should be. The same is true of memories #1 and #2. In order to correct this situation, the Tracking Counter must be allowed to go out of sync for the 80 shifts. This is done by not allowing it to count during the time the memories scroll. This reassigns the lines such that the spaces are in line 7. The bottom of Figure 2.8 shows the actual relationship between the data and the Tracking Counter. Note the Tracking Counter hasn't changed from the top reference.

Referring to the schematic, a scroll operation is initiated by ADV1* pulsing when the cursor is in the last line (LSTNE true), and ROLL is true. ADV* is blocked and flip-flop A7,5 is set true. This enables the D input of flip-flop A7,12. When ADDCOM is true, P1* strobes it and clocks flip-flop A7,9 true. This means that the character over the cursor is now at the output of memory #3. When this line (line seven) finishes shifting, the memories are in the position shown in Figure 2.8 at the top. That is, line 0 is ready to shift out. The end of shifting of line 7 is indicated when MCLKDS goes true. Since MCLKDS is inverted it has no effect on the state of flip-flop A6,9 until it goes negative again indicating the start of the next shift period. At this time A6,9 is inverted by C3,12 to become SCROL*, which sets up the memories as one shift registor when low. A6,8 being low clamps A7,5 and A7,9 low via AND gate A4,6. The signal READY is also held low which blocks any further inputs until the Scroll is completed. The reset input of flip-flop A6,13 is SCRLEN (Scroll Enable). This signal is generated on the VG/GT and is always a logical "1". The flip-flop A6,9 resets low ending the Scroll function when MCLKDS goes negative a second time at the start of another shift period.

2.4.2.4 Cursor Logic

The Cursor circuitry is in section C-2 of the schematic. Below this circuitry is a dual 4 line-to-1 line data selector, D8, with its inputs tied to GND. The two inputs SECT1 and SECT2 indicate which third of memory is being displayed. Pin 7 will be low for memory 1 display pin 6 and 5 low for memory 2 and 3 display. The 74155, F8, has its inputs for the half not used for LOAD* tied to GND also. The outputs are selected by A and B. E8 is a comparator which has an output, ENABLE, true when A and B equal SECT1 and SECT2. This indicates that the Video Generator is displaying the memory module that is selected by the Memory Address register which is the third of memory in which the cursor should be displayed. ENABLE enables the D input of flip-flop C1,2. When an ADDCOM (Address Comparison) is true during Scan Line 9 (S8 true) the character under which the cursor should be shown is being loaded into the Refresh. This sets flip-flop C1,5 true indicating that the cursor mark should be generated the next time S8 is true. C1,5 enables the D input C1,12. When S8 goes false C1,9 goes true enabling NAND gate D1,5. The next time S8 is true the second input of NAND gate D1,4 is enabled. Then when CHCOM (Character Comparison) goes true (after the trailing edge of P2*) B1,2 is enabled. The next P2* (one character delay later) sets B1,5 true making the cursor mark. Meanwhile, on the trailing edge of P2*, CHCOM went false allowing the flip-flop to reset on the third P2*. The cursor mark lasts for 639 nanoseconds or one character time.

2.4.2.5 Reset and Repeat Rate

In the lower left corner of the schematic, a 4 stage binary counter is driven by the Video Generator reset signal RST1 (60 HZ). This is divided by 4 to produce the 15HZ signal used for the repeat function on the keyboard. For the blinking cursor option the 4HZ output is used to clamp off the ENABLE signal at E8,3 (if jumper JP1 is installed).

When power comes on, the capacitor C10 charges more slowly than the power comes up causing A2,6 to be high and C2,6 to be low for a few milliseconds. This clamps the counter and the flip-flop B1 in the reset state. When C10 charges up, the inverters switch and release the resets. The buffered output of the flip-flop RST is used to cause a power clear of the memories by forcing the access circuitry to the clear function by setting A8,9 and A6,5 true as long as RST remains true. The Front End card also uses RST to condition the UAR/T and all flip-flops to the proper state. B1,9 goes true when the signal 4HZ goes true and returns false (250 milliseconds later) completing the reset function.

2.5 Detailed Description - Front End

2.5.1 Front End Block Diagram Description (Figure 2.9, page 2-45/46)

2.5.1.1 Serial to Parallel Converter

The converter is an MOS device called a UAR/T (Universal Asynchronous Receiver/Transmitter). It accepts parallel data and converts it to 10 or 11 bit serial data. It also accepts 10 or 11 bit serial data and converts it to parallel data. A clock is used to drive the chip and determines at what rate the device will operate. The clock has five switchable rates. The serial input and output is converted from TTL levels to either EIA (±13V) or current loop (20 ma) for operation with standard communication equipment.

2.5.1.2 Decode and Control Logic

Parallel data into the terminal (from the UAR/T) is checked for validity by the Decode logic. Characters from ASCII columns 2, 3, 4 and 5 are allowed into the memory. Characters from columns 6 and 7 (lower case) with the exception of Rubout are converted to columns 4 and 5 for input to memory. Control characters from columns 0 and 1 are ignored unless they indicate a terminal control function such as CR, LF, cursor controls, etc.

This logic generates the Access strobe and the cursor address control signals.

2.5.1.3 Keyboard Input

The keyboard supplies the only parallel input to the UAR/T. When a key is struck, the code along with a strobe is applied to the UAR/T for serialization. When the UAR/T has output the character another key may be struck. The only two keys on the keyboard not coded are BREAK and REPEAT. BREAK causes a 500 millisecond SPACE on the EIA output and is also used to control the Secondary Channel Request to Send, SCA. REPEAT is used to repetitively output the same code - 15 times per second (10 times per second for 110 baud).

2.5.1.4 RS232C Control Logic

The terminal is capable of operating on any 103 type Modem or 202 type Modem. For primary channel control the logic raises Request to Send (RQSEND) when the first character of a message is keyed and holds it true until an ETX (End of Text) character is output or a New Line function is performed (CR output in AUTOLF or LF in non-AUTOLF) at which time RQSEND is dropped. The terminal will wait until the Modem raises Clear to Send before actually outputting the first character.

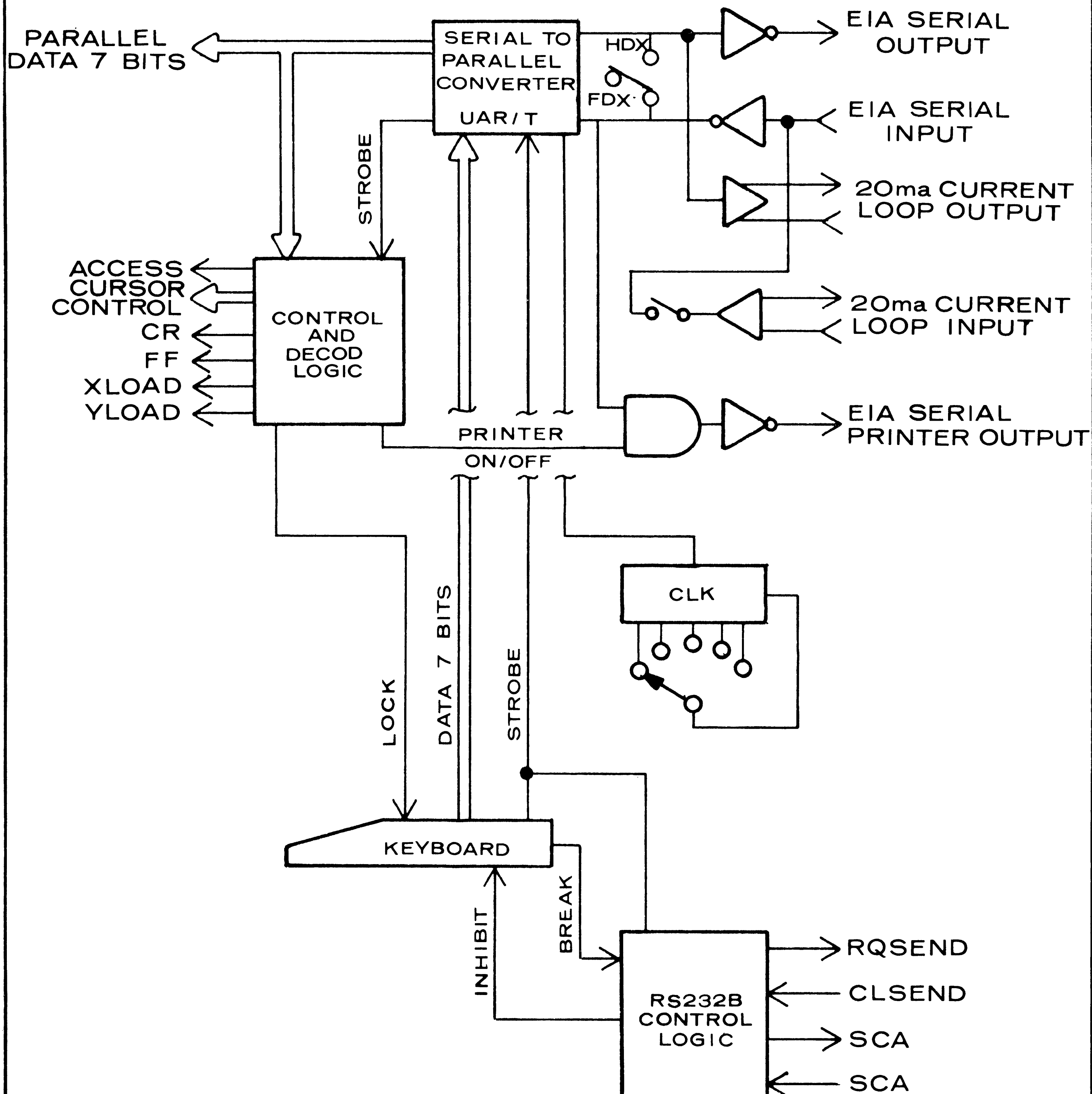
The Secondary Channel may also be controlled by the terminal. As a switchable option the keyboard will be locked until the computer allows the terminal to enter the send mode by use of the signals SCA and SCF. If the terminal is in the send mode the computer may interrupt and force it to the receive mode, locking the keyboard and resetting RQSEND.

2.5.1.5 Printer Output

There is a serial EIA output port for driving a serial printer. The output is enabled when a Printer-On code is received by the control logic. It is disabled with a Printer-Off code. When on, the printer output copies any serial data that the UAR/T would convert to parallel code. In Half-Duplex therefore the printer copies the keyboard data as well as data from the computer. In Full-Duplex only data from the computer is copied.

FRONT END BLOCK DIAGRAM

Fig. 2.9



2.5.2 Circuit Description - Schematic #135-079

2.5.2.1 Serial to Parallel Conversion

The UAR/T does the conversion from serial to parallel and parallel to serial at TTL levels. The serial data is asynchronous 10 or 11 bit. Normally the data line is at a true or 1 level until a character is sent. The start bit, always a zero, begins the character. The next seven bits are the data bits 1 through 7. The ninth bit is parity and the tenth or both the tenth and eleventh are stop bits, always 1's.

The UAR/T is driven by a clock that is 16 times the bit rate. The input is sampled by the clock for the first zero level. If a sample taken 8 clock periods later (center of start bit) is also low the rest of the bits are detected by center sampling and are stored in a latch. The stop bit (or bits) are checked as well as parity, if set. If all checks good the UAR/T raises Data Available, DA. If an error were detected, DA is still raised but either Parity Error, PE, or Framing Error, FE, are raised which results in NOR gate E3,13 being low. The Data out is on pins 6 through 11 of the UAR/T and is buffered for input to the terminal. If an error is detected E3,13 being low will force an asterisk code on B1 through B7. When DA goes true, AND gate output J8,8 goes true (E6,8 normally true) setting flip-flop E7,9 true. At the same time E6,12 is enabled so that the next positive edge of SCLK will set E6,8 false, which resets DA. The output data B1-B7 remains stable until just prior to the next DA true level. The edge of SCLK that set E6,8 true also clocked E7,5 true generating INSTB1 which generates ACCESS. E7,6 going false resets E7,9 so that the next SCLK pulse resets E7,5 low again completing one input cycle. This same SCLK pulse also sets E6,8 true again because DA has returned false.

In order to output a character the UAR/T must be presented a character in parallel and be given a strobe. When a key is depressed on the keyboard a 7-bit code is generated and applied to the inputs of the two quad latches A2 and B2. At the same time a strobe is generated called Keyboard Strobe, KBSTB. KBSTB when it goes true sets flip-flop C3,5 true (LOCK* is normally high and REPEAT is normally low). This enables the D input of flip-flop C3,12 and also strobes the latches to obtain B1L-B7L. When SCLK goes true C3,9 goes true which after a delay of 100 nanoseconds (R30, C14) resets C3,5 and removes the strobe from the latches. C3,8 has gone false and returns true on the next SCLK which strobes the UAR/T causing it to begin the serialization of the character. It is assumed that Clear to Send, CLSND, is true. If CLSND is false, DS is delayed until it goes true. The input REPEAT goes true when the Repeat key is held down causing a 15HZ signal at D3,9. If a character key is also held down D3,10 will be enabled and that character will be output at a 15HZ rate. If the character rate is too fast (15HZ at 110 baud for instance) the signal, Transmitter Buffer Empty (TBMT), will be low when the UAR/T is busy which forces C3,5 to be missed. The same will happen if characters are keyed too fast. The signal EOC, End of Character, indicates when the last stop bit for a character has been output.

There are several options concerning the UAR/T which are switch selectable. The Parity may be selected to be even or odd or always 1 or 0. When S6 is closed, the number of data bits is 7, plus one parity bit. The type of parity (odd/even) is selected by S7 which is on for odd and off for even. For no parity; S6 is left off which also selects 8 data bits. The state of the eighth bit is selected by S4; on for a zero, off for a one. The number of stop bits is selected by S5; on for one, off for two.

The clock is a differential comparator operating as a dual ramp integrator. The comparator is A8. The output (bare collector) is pulled up to +13V through 510Ω. When on, the output is near zero volts; when off the output is at the reference voltage of Zener diode D4 (5.1V). Assume A8 has switched from zero to +5.1V. This places the positive input pin 2 at +3.3V (note that the positive feedback network is biased at the other side by another Zener diode D3, also 5.1 volts). The output FCOM (Frequency Common) is returned to one of the five inputs FR1-FR5 through the baud rate switch on the rear panel. The capacitor C9 charges towards +5V. When +3.3 volts is reached the comparator switches low, changing the positive input to +1.65V. Now the capacitor discharges towards ground and again switches high when +1.65 Volts is reached. The inverter A7,2 inverts FCOM to generate SCLK which is the clock used by the UAR/T. The frequency is set by the five Cermet potentiometers R36, R38, R40, R42 and R44. The Baud Rate switch ties FCOM to FR1 for 110 Baud. The other points FR2-FR5, are 300, 1200, 2400 and 9600 baud. The frequencies are 1.76 KHZ, 4.8 KHZ, 19.2 KHZ, 38.4 KHZ and 153.6 KHZ respectively.

2.5.2.2 Decode and Control Logic

Input characters are screened by the decode logic to determine whether they are displayable, non-displayable or control functions. Bits four and five (B4 and B5) are decoded into four signals QDØ*, QD1*, QD2* and QD3*. These levels when low indicate in which quadrant of any pair of ASCII columns the character lies. If the character is a control character then CONTRL is true which when inverted by A7,8 enables the first 8 outputs of the BCD decoder, A5. Its outputs CDØ* through CD7* each go low for one of the possible combinations of B1, B2 and B3. Thus a combination of QDØ*-QD3* and CDØ*-CD7* can select any control character. This is done by use of NOR gates such as B5. For example, B5,1 is the Line Feed code (LF). The ASCII code for LF is 0001010. The first two zeroes are decoded by the NOR Gate D5,4 to enable A5. CD2* goes low because B3, B2 and B1 equal 010, or 2. QD1* goes low because bits 5 and 4 are 0 and 1 respectively. Therefore NOR gate inputs B5,2 and B5,3 are both low causing LF to be high. The other control codes used are generated in a similar manner.

The only exception to the decode method is RUBOUT which isn't in columns 0 or 1 and so must be handled differently. In section F-7, the output of NAND gate A3,8 is false when B1, B2 and B3 are true enabling NOR gate K6,2. For a RUBOUT QD3* is low which causes NOR gate K6,1 to be high enabling A3,3. When B6 and B7 are true then A3,6 is low causing J5,12 to be low blocking ACCESS and INSTB.

For cursor address two codes are used, VT and DLE. VT is used for Vertical positioning and DLE for Horizontal. The two flip-flops (L5) in section E7 and E8 control the addressing. For vertical address VT is true which enables the D input of L5,12 (L5,8 is true allowing AND gate J8,11 to go true with VT). The trailing edge of INSTB* sets L5,9 true and

L5,8 false. L5,8 being false blocks the ACCESS signal by forcing J5,12 low. This also blocks INSTB at E8,12. The AND gate J4,10 is enabled such that when the next input is made (flip-flop E7,5 pulses true) the signal YLOAD* pulses low. This in turn loads the least significant five bits of the character following VT into the line portion of the Address Register. The trailing edge of INSTB* resets L5,9 to false (pin 12 is low because L5,8 blocks AND gate J8,12) completing the function.

The Horizontal Address is done in the same way when DLE is input to the terminal. L5,5 now sets true generating XLOAD* causing the character following DLE to be loaded in the character portion of the Address Register.

The signals INSTB and ACCESS are blocked during the X and Y load periods because the address characters may be recognizable control or displayable characters.

The cursors are controlled by 5 codes from the ASCII control columns (0 and 1). The codes are:

HOME	SOH
→	ACK
←	NAK
↑	SUB
↓	LF

These are generated by the decode logic mentioned above. In section G-7 the logic array shown generates the pulses that are used by the Memory and Control board to move the cursor. Note that all five codes are strobed by INSTB to produce a clean signal. The Cursor Forward signal CURFR* is a combination of the forward code (ACK) and CURCK*, a signal from the access logic causing a cursor forward when an access to memory is made. The Cursor Up signal, UP*, is used in a special way. The logic in section H-7 is used to cause the cursor to go home to the bottom left in Roll mode by generating a cursor up after the home code is acted upon. When the code for cursor up is input,UP* pulses low causing CURUP* to pulse low via the AND gate H4,5. When a cursor home is done in Roll mode the trailing edge of the pulse HOME sets H5,9 true. The next SCLK pulse sets H5,5 true and H5,6 goes low resetting H5,9 again. H5,5 is combined with ROLL to produce a negative pulse at H5,8 causing CURUP* to pulse low. This causes the cursor to move from the HOME position (top left) up one line which causes a wraparound to the bottom left. If ROLL is false H4,9 is blocked and the cursor remains in the top left corner.

In the lower left corner of the schematic are two more control functions, Printer Enable and Keyboard Lockout. The signal RST* resets both J-K flip-flops (C7) upon power up. The Keyboard Lock flip-flop C7,13 (LOCK*) is optionally reset by the BREAK* signal or disabled by jumping J8,4 to ground. When enabled the code EOT causes LOCK* to go false blocking the Keyboard Strobe KBSTB at D3,13. STX sets LOCK* back true allowing the keyboard to operate again. When JP4 is inserted, the Break key may be used to unlock a locked keyboard. The other half of C7 controls the EIA Printer output. DC2 causes C7,9 to be high which enables AND gate D2,13 in section B-3. Any characters following will be output by the EIA driver F4,6. Note the input to D2,12 is the same as the serial input (inverted) to the UAR/T which means that the printer will copy whatever goes to the CRT screen in Full or Half-duplex.

2.5.2.3 <u>RS232C Interface</u>

The voltage range for the EIA standard RS232C interface is +3V to +15V for a Data zero level and -3V to -15V for a Data 1 level. Control signals such as Request to Send and Clear to Send have the same voltage swing but positive is true and negative is false.

Integrated circuits are available to translate these levels to TTL levels. The driver is a 1488 and the receiver is a 1489.

The EIA output signal, EIAOUT, is generated by F4,11 (1488). The UAR/T output is "ANDED" with BREAK* via D3,6 to drive F4,12 and 13. BREAK* goes false for about 1/2 second when the Break key is pressed causing a positive level (space) on the EIA output. The output of the UAR/T is normally high and goes low for space bits causing positive levels on EIAOUT. Another section of F4 (pins 4 and 6) is used for the serial EIA printer output described before.

The receiver F5 (pins 4 and 6) is a section of a 1489 and has a TTL level output. EIAIN is converted to TTL and applied to NAND gate B3,5 for input "or-ing" to the UAR/T. If the signal HDX (Half Duplex) is false B3,9 is blocked and output data D3,6 is not gated into the UAR/T. If HDX is true then serial TTL output data is mixed with the input data to provide a local echo path. Either data from the CPU or the keyboard will be input to memory. Switch S1 connecting the output of NAND gate B3,3 to the input of B3,4 blocks the input when Request to Send is high in Half-Duplex mode to supress any echo from the external device (202C modem for instance).

The Request to Send circuitry is just above. When a key is struck, the RQOUT* goes low (C3,6 in section C-5) which sets E6,5 true and RQSND* false which via F4 drives RQSND true. The modem raises CLSND which when converted by F5,3 (Section C-5) allows the character to be output. RQSND remains true until an ETX, CR (AUTO LF) or LF (non-AUTO LF) is output. The flip-flop (section D-1) is set when E8,4 is true and EOC (End of Character) returns true. E8,4 is true for three conditions. Assuming JP1 and JP2 are installed, one condition is the output of ETX which when true drives H6,8 false and E8,4 true via D7. When F7,6 goes true (pin 2 grounded, F7 was preset by E6,5 being low before the process began) the signal SCLK/16 (SCLK divided by 16) clocks the flip-flop F7,8 false and then true which clocks E6,5 back low completing a Request to Send sequence. If the terminal is in AUTO LF then the CR code enables E8,4. In non-AUTO LF the LF code enables E8,4.

The NOR gate E3, 1, 2 and 3 is used to generate ATOLFG used by the Memory and Control for Erasing in non-AUTO LF mode. This is done by forcing AUTO LF true when CLRFF goes true during an Erase function.

2.5.2.4 Reverse Channel Control

The Reverse Channel (202C) control circuitry is in section F-3. If the reverse channel is to be used for circuit assurance and interrupt, Switch S3 should be closed. Upon power up or after a transmission, flip-flop C8,9 will be true forcing TRANS low blocking any keyboard input by clamping flip-flop C3,5 reset (Section C-5). At the same time since BREAK is false and C8,8 is false, SCA is true. SCA is the signal that causes a 202C modem to turn on the reverse channel carrier. The CPU monitors SCA for a negative condition and holds SCF normally false. SCF is the received signal detector for the reverse channel. When the user presses the Break key the signal BREAK goes true for approximately 500 milliseconds driving SCA false. The CPU detects the negative level on the reverse channel and responds by raising and dropping carrier or just dropping carrier if already raised. The trailing edge of BREAK sets flip-flop C8,5 true, conditioning the clock input of C8,11 to follow the Carrier Detect signal CARDT1. When the carrier goes false flip-flop C8,9 goes false which enables NOR gate K6,5. When SCF goes true (CPU raises SCA at its end which is SCF at the terminal) K6,6 goes false causing TRANS to go true enabling the keyboard strobe. (Note that the break signal when going true causes a negative pulse of approximately 100 nanoseconds at J5,5 presetting C8,9 true. This allows the transmit mode to be aborted with a Break.) When the transmission is complete Request to Send returns false causing RQSND* to go true which places a 100 nanosecond negative pulse at J5,4 which presets C8,9 forcing TRANS back false. (H8 is a 74121 one-shot. The time constant is determined by R12 and C10, C11).

2.5.2.5 Current Loop

The Current Loop portion is in the lower right hand section. L7 and K8 are opto-isolators (MOC1000). The input stage is K8. When current is present K8,4 and 5 present a low impedance to -13V. Q5 is turned on holding the EIA input to approximately -11V (S2 is closed for current loop operation). When the loop opens (space) K8,4 and 5 present a high impedance and Q5 turns off allowing the EIA input to go to +13V. The diodes D11 and D10 are used to keep Q5 from saturating insuring that the output stage of K8 is not in an overdrive condition which would reduce the speed because of excess minority carrier storage.

The output stage also uses a opto-isolator (L7). When in the mark condition Q3 is on (because D3,6 is high) which turns on the output stage of L7, Q4 is also on supplying a low impedance to the loop. The diodes D5 and D6 are used to keep Q4 from saturating for the same reason as the input stage. The other two diodes D7 and D8 are to insure some bias voltage for the base of Q4. When a space condition occurs Q3 turns off (D3,6 low) which in turn causes Q4 to turn off, opening the loop.

The diodes across the input and output, D12 and D9, are to protect the circuits from reverse voltage.

2.5.2.6 Miscellaneous

The carrier light is driven by the discrete circuit in section H-4. Normally D2 is not installed. When the Carrier Detect signal goes true (Section E-4) CARDT1 goes true which turns on Q1. Q1 turning on also turns on Q2 and supplies +13V through 300Ω to the lamp. The other side of the lamp is referenced to -13V.

Units delivered after January 15, 1974 have alarm circuitry (Section E5 and 6) which activates a "Sonalert" alarm upon receipt of a BEL code producing an audible tone for approximately 1/2 second. The BEL code is decoded by E3,4 from QDO* and CD7*. L3 is a one-shot that pulses for a period determined by R50, C15 and C16, starting on the leading edge of INSTB if L3,3 is true. Q6 amplifies the pulse from L3,6 to drive the "Sonalert."

The two signals DATTRY (Data terminal Ready) and LBIAS (Loop Bias) go to the output connector. DATTRY is needed by a modem when EIA levels are used. DATTRY and LBIAS may be used in a current loop connection to supply the current.

The straight through connections shown in Section D-6 carry I/Ø signals to the back plane for use by other cards.

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3. GLOSSARY OF SIGNAL NAMES

A,B - Select Address for memory module [Source-C3, VG]; 2 stage counter, tracks memory module for desired address (i.e., cursor position)

ACCESS - Gated INSTB1 [Source-D7, FE]; inhibited by address advance, all control except FF and CR.

ADDCOM - Address Comparison [Source-B4, VG]; CHCOM and line counter comparison.

ALARM* - Pulses terminal bell equivalent, [Source-E5, FE].

ADV* - Advances line address counter [Source-B2, MC].

ADV1* - Cursor crossed line boundry [Source-C6, VG].

ATOLFG - Allows memory and control to erase in non-auto LF mode [Source-E3, FE].

BREAK - 500 ms. pulse derived from BREKEY, [Source-F4, FE].

BREKEY - Break Key, [Source-Keyboard].

BX(X = 1 to 7) - Gated out buss of UAR/T, [Source-D3,FE]; output of UAR/T.

BXL(X = 1 to 7) - Latched keyboard data, [Source-C7, FE]; latched by gated KBSTB.

BXV(X = 1 to 6) - Output of refresh memories, [Source-F1, MC].

C1LR,C2LR - P1* and P2* gated with MCLKDS, [Source-A5, MC].

C1RR, C2RR, - Buffered P1* and P2* for driving refresh memories [Source-D1, MC].

CARLT - Carrier Light, [Source-G3, FE]; activates CARRIER light on terminal.

CHCOM - Character Comparison, [Source-C6, VG].

CLK - Main signal clock, [Source-H6, VG]; 12.528 MHZ

CLR1,2,3 - Load space code (all zeros) into display memory, [Source-H7, MC].

CLRG - Load space code (all zeros) into display memory, [Source-H7, MC]; used on units after January 15, 1973.

CLSND - Clear to Send, [Source-MODEM]; allows terminal to input characters.

CMBSN* - Combined Sync, [Source-F3, VG]; includes VDRIVE and gated HDRIVE (8 character times after HDRIVE).

COMENB - Comparison Enable, [Source-E2, VG]; inhibits CHCOM during memory pause and synchronization.

CR - Carriage Return, [Source-G5, FE]; decode from keyboard.

CURBK* - Cursor Back, [Source-G7, FE]; back code (NAK) gated with INSTB.

CURCK* - Cursor Clock, [Source-F6, MC]; advances cursor one position.

CURDWN - Cursor Down, [Source-F7, FE]; down code (LF) gated with INSTB.

CURFR* - Cursor Forward, [Source-G7, FE]; equals CURCK or forward code (ACK).

CURUP* - Cursor Up, [Source-H6, FE]; equals up code (SUB) or after HOME (Roll Mode) a pulse to position cursor in the bottom left.

D4* - One character time, [Source-H5, VG]; 1.566 MHZ (639 nsec).

DA - Data Available, [Source-D4, FE]; output of UAR/T.

DATAGT - Data Gate, [Source- G4, VG]; 80 character time signal, gates data, set at count 15, reset at 95, starts one character before data is displayed on screen.

DS* - Data Strobe for UAR/T, [Source-C4, FE]; parallel data available to UAR/T.

EIAIN - Input from MODEM, [Source-MODEM].

EIAOUT - Output to MODEM, [Source-C2, FE].

ENABLE - A,B, equals SECT 1,2 [Source-B2, MC].

EOC - End of Character, [Source-C4, FE]; from UAR/T, last stop bit outputted.

FCOM - Frequency Common, [Source-B5, FE]; to common of baud switch.

FE - Framing Error from UAR/T, [Source-C3, FE].

FF - Form Feed, [Source-H5, FE]; decode from keyboard, same as screen erase.

FR1,2,3,4,5 - Inputs from baud switch, [Source-Baud Switch].

HBLANK - Horizontal Blank, [Source-G2, VG]; set at character count = 97, reset at 15.

HDRIVE - Horizontal Drive, [Source-F1, VG]; used by internal monitor, set at HBLANK, reset at character count = 31.

HOME - Home code during INSTB, [Source-G7, FE].

INSTB1 - In strobe, [Source-E5, FE]; function of selected baud rate.

KBSTB - Keyboard Strobe, [Source-Keyboard]; data available from keyboard.

KXKB (X = 1 to 7) - Keyboard Data, [Source-Keyboard].

LOAD* - Strobe for input to display memories, [Source-F6, MC].

LOCK* - Keyboard locked signal, [Source-B7, FE]; from EOT to STX.

LRCLK - Advances memory tracking registers, [Source-E6, MC]; equals C2LR, gated off during scrolling.

LSTLNE - Last Line, [Source-D5, VG].

MCLKDS - Memory Clock Disable, [Source-D2, VG]; equals COMENB*, allows for sync during video vertical flyback.

MEOL* - Memory End of Line, [Source-B6, VG]; display memories have shifted 80 counts.

P1,P2 - Buffered inversion of P1* and P2* for driving display memories [Source-B4, MC]; gated with MCLKDS.

P1*,P2* - Two-phase Clocks for one character position, [Source-G5, VG].

PE - Parity Error from UAR/T, [Source-C3, FE].

RDA* - Reset DA in UAR/T, [Source-D5, FE].

READY - Access logic not busy, [Source-E7, MC].

REPEAT - Output of keyboard Repeat key, [Source-Keyboard].

RQSND - Request to Send, [Source-D2, FE]; signal to MODEM indicating terminal ready.

RST - Power on reset, [Source-C6, MC]; occurs once per power up sequence.

RST1 - Half character pulse at line count = 29, [Source-G2, VG]; resets line counter.

S8 - Ninth scan line, [Source-H3, VG].

SCA - Secondary Request to Send, [Source-E2, FE]; normally true, low during BREAK, acts as interrupt to MODEM.

SCF - Secondary Rec'd Line Signal Detector, [Source-202C MODEM]; terminal uses to determine permission to transmit.

SCLK - 16 times UAR/T bit rate, [Source-D5, FE]; function of selected baud rate.

SCRLEN - Scroll Enable, [Source-D2, VG]; equals DATAGT and sync FF (set RST1, reset end of VBLNK).

SCROL* - Forces display memories to scroll, [Source-E6, MC].

SECT1,2 - Select Memory Module, [Source-E4, VG]; 2-stage counter, clocked at data line 11 and SL1, and data line 19 and SL1. (60HZ)

SFCLK - Static memory clock, [Source-G5, MC]; pulse stretched CILR.

TBMT - Transmitter Buffer Empty [Source-C4, FE]; from UAR/T, necessary before sending DS.

VBLNK - Vertical Blank [Source-F1, VG]; set SL1 and data line 28, reset SL9 and data line 3 (60HZ)

VDRIVE - Vertical Drive, [Source-E1, VG]; set RST1, reset data line 1, used by internal monitor.

XLOAD* - Similar to YLOAD, [Source-E7, FE]; loads into character portion, provides for cursor character advance.

YLOAD* - Loads least significant 5 bits of character following VT into line portion of address register, [Source-E7, FE]; provides for cursor line advance.

4. UNIT TEST PROCEDURE

The off-line test procedure described in this section provides assurance that the terminal is operating properly. We shall assume, before the steps below are followed, that no cables are plugged into the Data Connector on the rear panel of the 580 and that the unit is set up for EIA operation (Switch #2 on the FE/GT card placed to the OFF position.)

a. Place the POWER switch ON; the red indicator should light and the screen should show a clear white rectangular "display page" after approximately a 30-second warmup, with the cursor at the top left corner of the page.

   [If the red indicator does not light, check the line cord. If the cord is properly connected and you have ascertained that the wall receptacle contains power, the fuse on the rear panel should be checked. The fuse is type 3AG, 1.5 Ampere, SLO-BLO.]

b. Place the ROLL and AUTO LF switches in the depressed state. Place the FULL DUP switch in the non-depressed state.

   1) Key [ABDHP (SP)], where (SP) = space

      [At this point you may wish to readjust the TV picture by using the BRITE and CONT controls on the rear panel. For proper adjustment first back off both controls fully so that no picture is visible. Bring Brightness up until a raster is visible, then carefully back off Brightness to the point that the raster lines are just not visible. Finally bring up Contrast to the desired level for a clear picture.]

   2) Key [KcK], where Kc = Control-K
      The cursor should move vertically down to about the center line.

   3) Key [ABDHP (SP)]

   4) Key [KcW]
      The cursor should move vertically down to the bottom line.

   5) Key [ABDHP (SP)]

   6) Key [NEW LINE]
      The cursor should go to the bottom left corner and all data should scroll up one line.

7) Key [PcYs], where Ys = Shift-Y
The cursor should go to right bottom corner.

8) Key [LF], until the bottom ABDHP is in the top line- (a flash of ABDHP elsewhere is normal during a scrolling operation).

9) Key [PcPcs], where Pcs = Control - Shift-P
The cursor should return to the left margin.

c. Place the ROLL switch in the up position.

1) Key [NEW LINE]
The cursor should go to the top left corner.

d. Place AUTO LF in the up position.

1) Key [NEW LINE]
The ABDHP should be erased in units delivered prior to January 15, 1974 and the cursor remain in the top left corner. In units delivered after January 15, 1974 the ABDHP should not be erased.

2) Key in a few characters and then depress CONTROL and SCREEN ERASE - the screen should erase.

e. Depress the FULL DUP switch.

1) Key characters - none should go on screen.

2) Return to Half-Duplex (FULL DUP up)

f. Check that all keys on the keyboard work (except PRINT ON and PRINT OFF, unless a serial printer is attached to the Printer port). Note that SCREEN ERASE works only when the CONTROL key is held down.

g. Place the unit in ROLL mode.

Check that HOME is bottom left.

h. Place the unit in non-ROLL mode.

1) Check that HOME is top left.

2) Using the REPEAT key, enter a line of characters and note that the cursor advances to the next line when the current line is completely filled, for units delivered after January 15, 1974. [For units delivered prior to that date, the cursor goes back to the beginning of the same line.]

i. Return to ROLL mode.

Move cursor down with [↓] and check that the screen scrolls only when the cursor in in the bottom line.

j. Press the Control-G combination on the keyboard and note that the audible alarm sounds. [Note: The alarm is available only on units delivered after January 15, 1974.]

k. To check the printer output, wire a serial EIA printer to the Printer output connector.

1) Key in characters - they should not go to the printer.

2) Key [PRINT ON]
All characters keyed should now go to the printer as well.

3) Key [PRINT OFF]
Characters should no longer go to the printer.

Note: In place of a printer an oscilloscope may be used to observe that the output level at the Printer connector (-13V) pulses to +13V when characters are keyed during the Printer On portion of the test procedure.

If all of the above are operative, you are ready to start on-line operation.

Two further tests may also be performed if one wishes to test the EIA driver/receiver circuits and the opto-isolator used for current loop operation:

1. To check the EIA driver/receiver.

Connect a wire from pin 2 to pin 3 of the 25-pin data connector and check that data is keyed to the screen when in Full-Duplex.

m. In order to check current loop the shroud must be removed and switch no. 2 on the FE/GT card placed ON.

1) At the data connector, connect a wire from pin 22 to 24, connect 25 to 17, and connect 18 to 7.

2) Key data in Full-Duplex and check that data goes to the screen properly.

Note: If you wish to operate off-line without jumpers (or EIA), switch #2 on the FE/GT card must be set back to OFF.

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5. PHYSICAL ACCESS FOR TEST AND REPAIR

5.1 Controls, Indicators and Connectors

A detailed description of the function of all controls and indicators, and of interface connections is given in ADDS publication 58-3000, How to Use the Consul 580. At this point we shall simply summarize those components.

Controls and indicators on the front of the Consul 580 are:

- An ON-OFF pushbutton power switch.
- A POWER indicator lamp. (Red) This is in series with a fuse in the primary of the power supply transformer.
- A CARRIER indicator lamp. (Yellow) This lamp indicates that the signal "Carrier Detect" is high.
- Three Mode Select pushbuttons. These switches permit selection of FULL DUP, AUTO LF, or ROLL mode.

Located on the rear panel (Figure 5.1) are:

- Data connector. This is a 25-pin female Cinch or Cannon type DB 25-S. A mating connector (Cinch or Cannon type DB-25 P) is supplied with terminals.
- BNC Video Output connector. This is used to connect 75-ohm coaxial cable (RG 59/U or equivalent) for driving slaved external monitors.
- PRINTER 4-pin plug. Used to connect a serial printer.
- A 1.5 Ampere "SLO-BLO" fuse.
- A 3-pin power cord connector. The "device" end of the removable Consul power cord plugs into this connector.

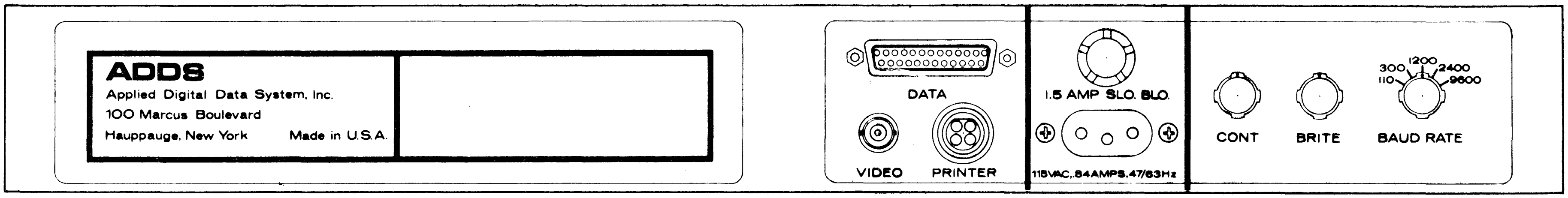
Do not plug 115 volt terminals into a 230 volt outlet.

Consuls may be supplied to operate on 230V/50HZ.

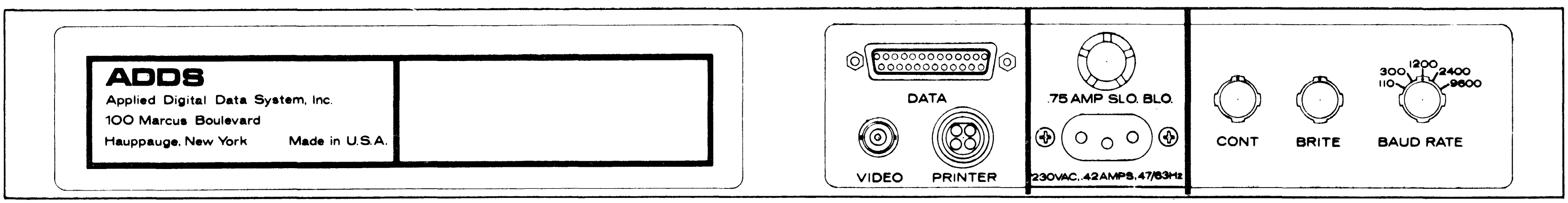
- A 5-position BAUD RATE switch. This switch is used to select the desired serial baud rate. Speeds of 110, 300, 1200, 2400, and 9600 baud are standard on the Consul. Other baud rates are available on special order.
- BRITE control knob. Sets TV screen brightness.

CONSUL 580 REAR PANEL

Fig.5·1



REAR PANEL 115VAC



REAR PANEL 230VAC

- CONT control knob. Sets TV screen contrast.

5.2 Access to PC cards and Subassemblies

The top shroud of the Consul is removed to service the PC cards and subassemblies. To take the shroud off, remove four Phillips head screws; two at the lower front corners of the terminal and two at the top rear corners. Then tilt the shroud slightly to the rear and left it off. (See Figure 5.2)

Figure 5.3 shows the 580 with its shroud removed. The item numbers in Figure 5.3 are referenced in the following paragraphs.

Note the four fasteners (#8) by which the shroud is attached.

The majority of service problems involve only removal and replacement of PC cards. The layout of PC cards within the card cage (#6) is shown in Figure 5.4. The two hold-down brackets (#5) must be removed before PC cards can be changed. Cards may be removed by grasping the end firmly and working the card up and down while exerting a pulling force. For those personnel who must remove cards frequently a "card puller" is recommended. (ADDS service personnel use the "Wire-Grip" puller, part #1733, made by E.H. Titchener and Co., 1 Titchener Place, Binghamton, New York.)

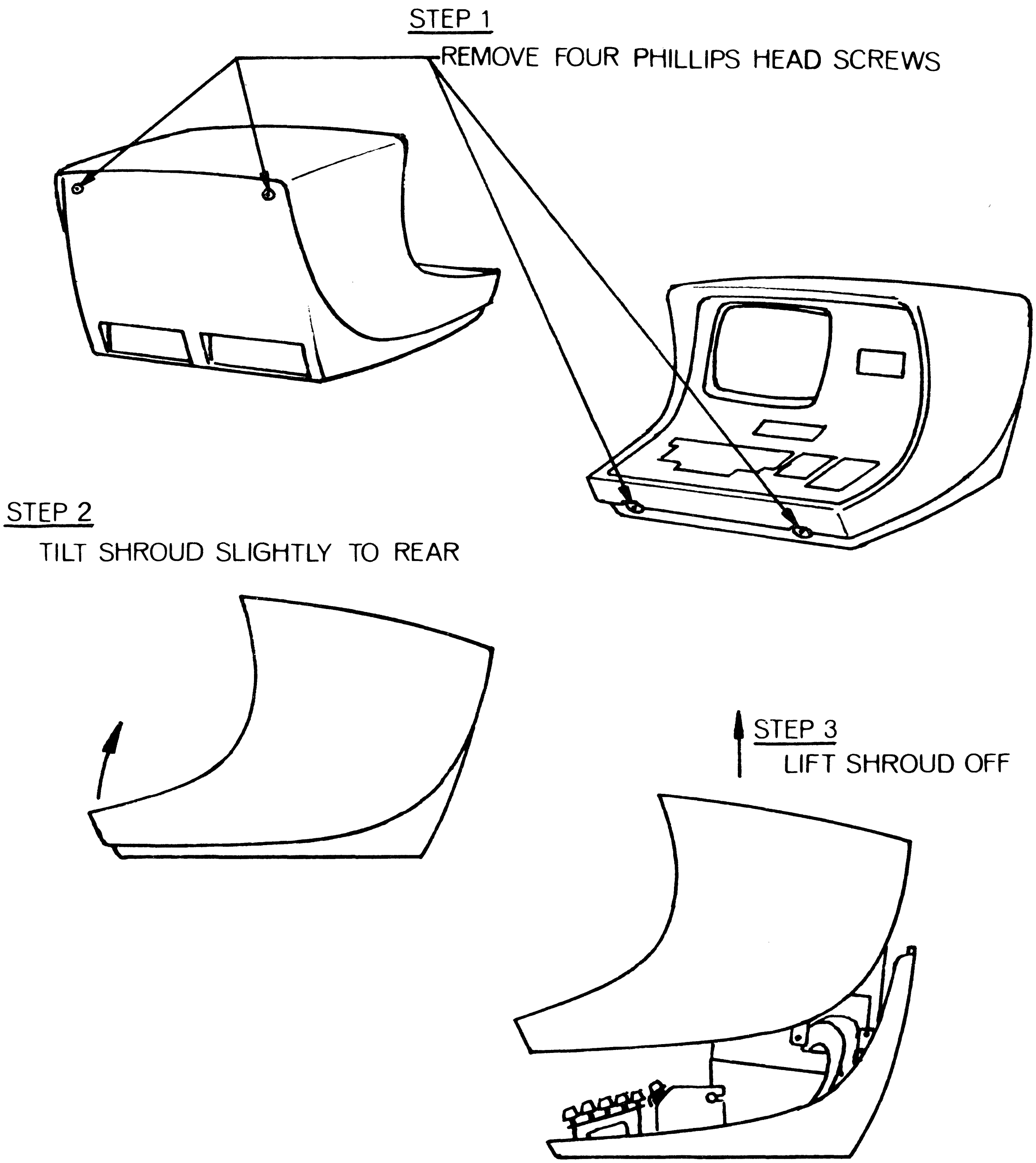
When cards are inserted they should be pushed in until the card shoulder firmly seats against the backplane connector. Cards will not come loose in normal shipment and use since they are firmly seated with long fingers and held in place. However, if the performance of the device is erratic after shipment (or very rough handling is suspected) the cards should be inspected to insure that all are firmly seated.

When the terminal is "unbuttoned" as in Figure 5.3 power may be applied and the device operated if one wishes to check signals in the cabling, the PC card backplace, connector terminations, etc.

If circuitry is to be checked with an oscilloscope as the terminal is operated, an ADDS extender board should be plugged into a card slot and the card plugged into the end of the extender card. The ADDS extender card has a center ground plane to prevent signal pickup and interference between signals on the two sides of the extender. The extender card is almost a necessity if one wishes to diagnose faults to the chip level, rather than the card level. The alternative for chip-level repair is to sequentially re-

SHROUD REMOVAL

Fig. 5-2

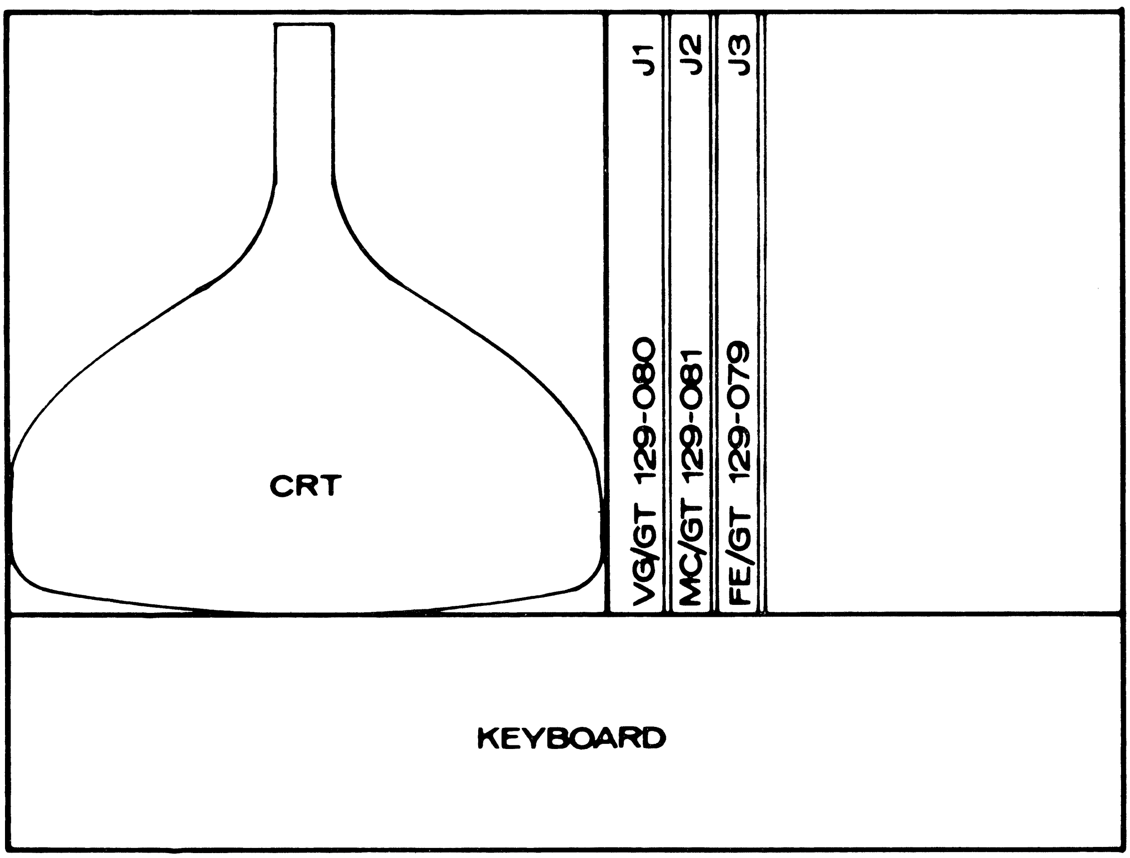


CONSUL 580 WITH COVER REMOVED

Fig.5-3

CONSUL 580, P. C. CARD LOCATIONS

Fig. 5-4



—TOP VIEW—

place the suspect chips on a card, if fault isolation is performed only to a card level.

Occasionally subassemblies must be removed, rather than simply changing PC cards. Various subassemblies are discussed below, with item numbers referencing Figure 5.3

CRT monitor To remove, undo 3 nuts (#1) and disconnect the connector on the back edge of the monitor P.C. card, and the "Molex" connector which brings power to the monitor subassembly. The monitor can now be lifted out.

Keyboard (#2) To take the keyboard out remove the screws at each end which secure it to the mounting brackets. Next disconnect the P.C. Board connector on the front of the unit. The keyboard can now be removed.

If when you replace the shroud on your unit any of the keys on the periphery of the keyboard bind on the opening in the shroud, lift the front of the terminal up and loosen the 4 keyboard mounting screws. Now position the keyboard so that there is an even clearance between the keytops and the opening and then tighten the 4 mounting screws. This adjustment should not normally be necessary unless a new shroud is installed.

Power Supply (#3) To remove, take off the power supply cover (#10), the card cage (#6), and remove the keyboard (#2), and disconnect the harness from the terminal strip on the power supply. Now lift up the front of the terminal so that you can see the underside of the unit. Remove the 4 countersunk screws near the hole for the fan and set the unit down. You may now slide the power supply out the front, twisting it slightly as you do to clear the keyboard mounting bracket.

Card Cage (#6) To remove take out the 2 screws on the outside of the card cage and loosen the 2 screws on the side closest to the monitor. Now slide card cage forward and lift up. The harnesses are long enough so that the card cage can be laid next to the terminal with the backplane accessible. To disconnect the harness from the card cage remove hold down brackets on either side of the access window and pull out connectors.

Lamp and Switch bracket (#4) To remove, lift up the front of the terminal until you can see the bottom. Remove 3 screws and the mounting plate and set the unit back down. Now lift the bracket up and lay it on top of the keyboard. Disconnect the harness from the terminal strip and remove the assembly.

Backpanel (#9) The chassis supporting the CRT and the card cage must be removed. Five screws, 2 on each end and one in the middle must be removed; then disconnect the CRT connector and the connectors to the card cage. Then lift the entire chassis assembly out. You can now access the back panel.

5.3 Controls, Indicators and Connectors for the MRD-380

Controls and indicators on the front of the MRD 380 are:

- An ON-OFF toggle power switch.

- A POWER indicator lamp. (Red) This is in series with a fuse in the primary of the power supply transformer.

- A CARRIER indicator lamp. (Yellow) This lamp indicates that the signal "Carrier Detect" is high.

Located on the rear panel (Figure 5.5) are:

- Data connector. This is a 25-pin female Cinch or Cannon type DB 25-S. A mating connector (Cinch or Cannon type DB-25 P) is supplied with terminals.

- BNC Video Output connector. This is used to connect 75-ohm coaxial cable (RG 59/U or equivalent) for driving external monitors.

- Three Mode Select toggle switches. These switches permit selection of FULL DUP, AUTO LF, or ROLL mode.

- PRINTER 4-pin plug. Used to connect a serial printer.

- A 1.5 Ampere "SLO-BLO" fuse.

- A 3-pin power cord connector. The "device" end of the removable Consul power cord plugs into this connector.

  Do not plug 115 volt terminals into a 230 volt outlet.

  Consuls may be supplied to operate on 230V/50HZ.

- A 5-position BAUD RATE switch. This switch is used to select the desired serial baud rate. Speeds of 110, 300, 1200, 2400, and 9600 baud are standard on the Consul. Other baud rates are available on special order.

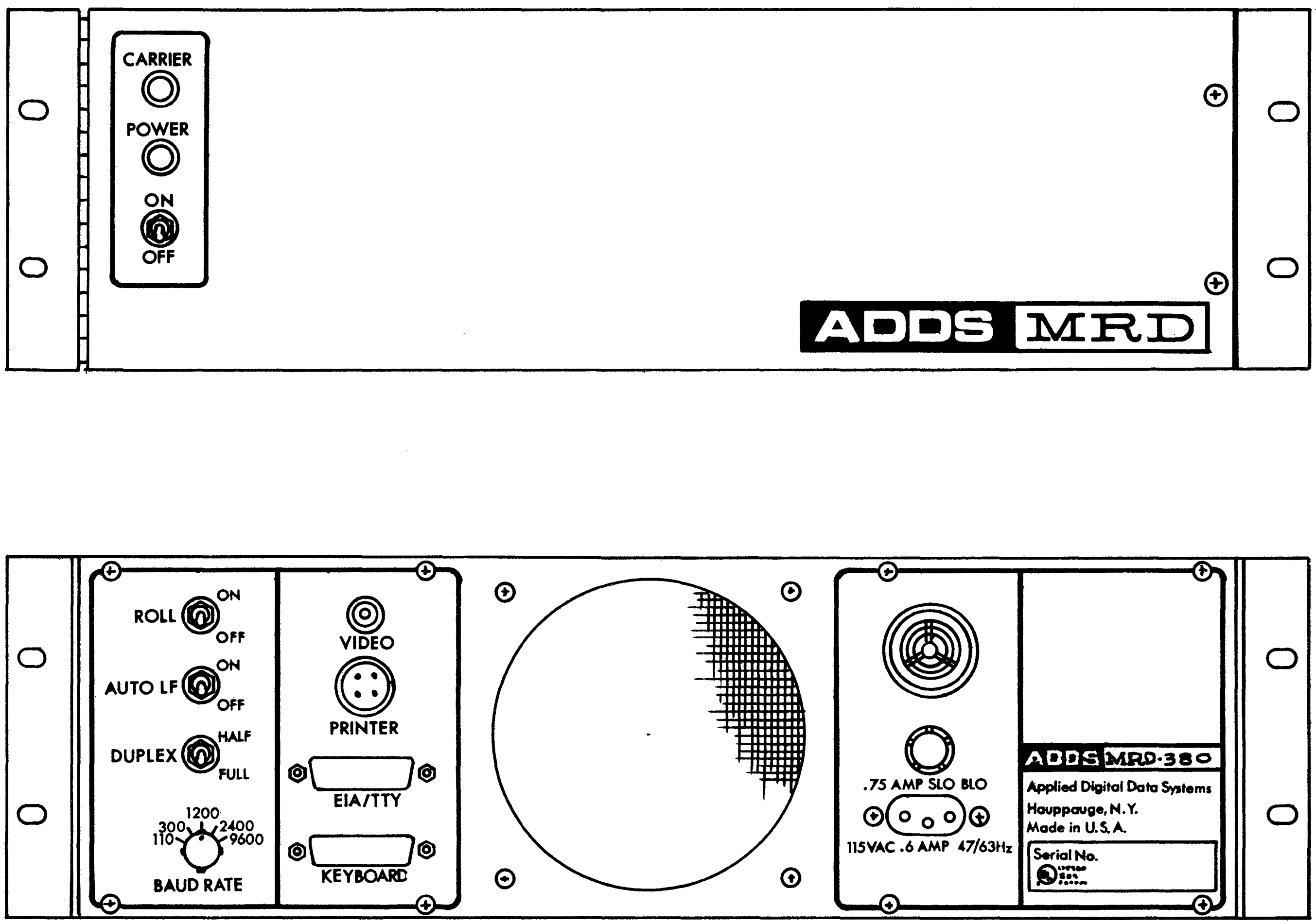
5.4 Access to PC cards and Subassemblies

The front door of the MRD is opened to service the PC cards and subassemblies. The majority of service problems involve only removal and replacement of PC cards. The layout of PC cards within the card cage is shown in Figure 5.6. Cards may be removed by grasping the end firmly and working the card up and down while exerting a pulling force. For those personnel who must remove cards frequently a "card puller" is recommended. (ADDS service personnel use the "Wire-Grip" puller, part #1733, made by E.H. Titchener and Co., 1 Titchener Place, Binghamton, New York.)

When cards are inserted they should be pushed in until the card shoulder firmly seats against the backplane connector. Cards will not come loose in normal shipment and use since they are firmly seated with long fingers and held in place. However, if the performance of the device is erratic after shipment (or very rough handling is suspected) the cards should be inspected to insure that all are firmly seated.

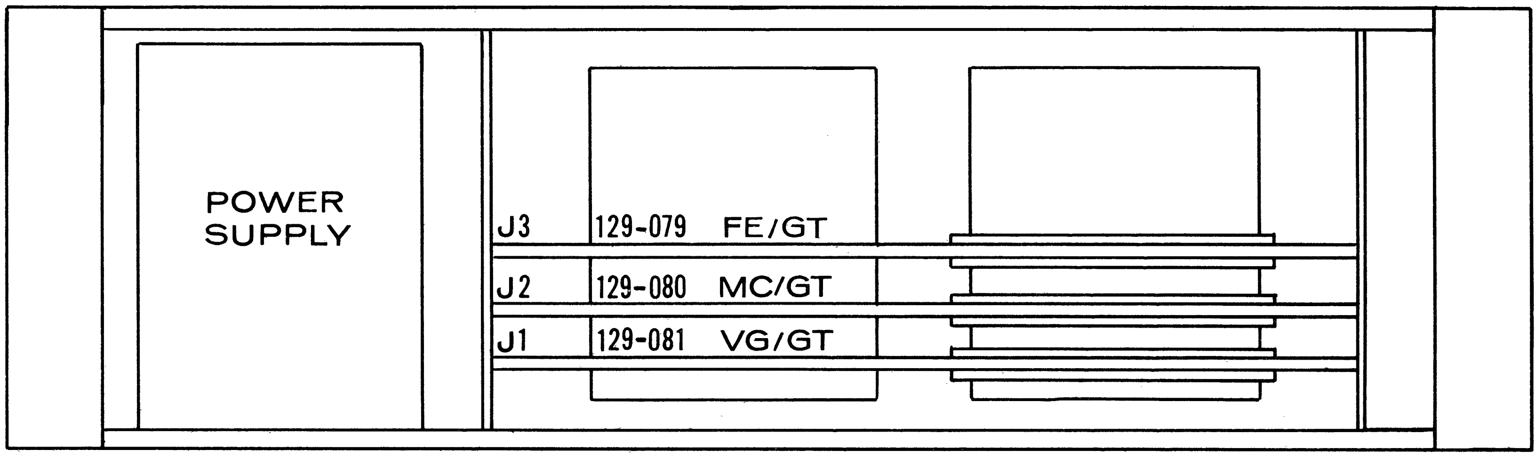
MRD 380 FRONT & REAR PANEL

Fig. 5·5



MRD 380 PC CARD LOCATOR

Fig 5.6



– FRONT VIEW –

6. TROUBLE-SHOOTING CHART

A trouble-shooting chart is presented, to the module replacement level. All possible faults can obviously not be listed, but fault diagnosis to the suspect module(s) or subassembly will be facilitated by reference to the chart.

In cases where the cause of a symptom cannot be summarized in a brief phrase the column labeled "Probable Cause" has no entry, but the module(s) or subassembly to be replaced is listed.

Turn Power OFF before removing or inserting a Printed Circuit card.

It is essential that, if a defective card has apparently been found, it be reinserted to verify that the symptoms reappear. If the symptoms do not reappear, the fault could have been corrosion on edge connector contacts or a temperature sensitive I.C. chip. It may be necessary to bring the device back to the operating temperature at which symptoms were first observed to find such chips.

On page 6-2 a list of equipment and parts for servicing to both the module replacement level and the chip level is given.

SERVICE EQUIPMENT AND PARTS

Minimum and Optional

Spare Parts

1. PC Cards (Card complement per Locator Chart in Section 5.)
2. $1\frac{1}{2}$ amp Sloblow fuse
3. Power Supply - optional
4. Spare chips - optional

Tools

1. Phillips head screw driver, medium and small, w/long shank
2. Flat screw driver, medium and small
3. Card extractor
4. Video monitor
5. Extender card - optional
6. Cutters - optional
7. Pliers - optional
8. Soldering iron/solder - optional
9. Solder wick - optional
10. Oscilloscope - optional
11. Trouble lite - optional
12. VOM - optional
13. Frequency counter - optional

TROUBLE-SHOOTING CHART

Trouble	Probable Cause	Remedy or Bad Board
Power Light fails to come on when Power On switch pressed	a) AC power b) fuse c) faulty switch d) faulty light	a) check receptacle b) replace 1½ ampere "sloblo" fuse c) replace switch d) replace lamp
Fan fails to come on when Power lamp is ON.	a) faulty fan	a) replace fan
Picture fails to appear after warm-up time. Power light and fan OK.	a) poorly adjusted contrast or brightness b) poorly seated P.C. cards c) d) power supply faulty	a) adjust contrast and/or brightness b) remove shroud (open MRD-380 panel) and check card seating c) VG/GT card d) check for shorts or replace supply
Picture fails to appear on screen but does appear on external monitor	a) poorly adjusted contrast or brightness b) c) faulty Brightness or Contrast pots d) loose connector on monitor	a) adjust controls b) remove shroud (Consul series) and replace P.C. card on internal monitor chassis c) replace pots d) remove shroud and check connector on rear of monitor (Consul series) e) VG/GT card
Screen comes up blank after Power ON and no characters may be entered, but cursor moves when characters keyed		a) MC/GT card b) FE/GT card c) VG/GT card

Trouble	Probable Cause	Remedy or Bad Board
Screen comes on full of random characters	a) Power on reset circuitry faulty b) Power down too short	a) replace MC/GT b) cycle power Sw.
Unit gets hot and shuts down	a) blocked fan b) stopped fan c) power supply malfunction or thermal cutoff	a) clear b) clear or replace c) replace power supply
All " " on screen "?" or "@" on 1/3 or more of screen		a) VG/GT card a) MC/GT card
Characters distorted by extra dots in character field	b) low +5V supply	a) VG/GT card b) adjust +5V or replace
Characters aren't recognizable but may be altered by keying from keyboard	b) low +5V supply	a) VG/GT card b) adjust +5V or replace
All positions on screen appear black w/narrow white borders		a) VG/GT card
Certain groups of characters can't be entered on screen		a) FE/GT card b) VG/GT card c) Keyboard replacement
Black vertical line appears in middle of screen with data running up screen		a) VG/GT card
Screen torn and distorted	b) faulty monitor c) 50 or 60 cycle operation jumpers incorrect	a) VG/GT card b) replace monitor c) correct as per description on VG/GT schematic

Trouble	Probable Cause	Remedy or Bad Board
Characters have missing horizontal lines		a) VG/GT card
Characters appear in Right or Left margin		a) VG/GT card
Page on screen wrong in horizontal or vertical size		a) VG/GT card b) adjust TV monitor
Cannot move cursor		a) replace keyboard b) VG/GT card c) MC/GT card
Cursor moves erratically	b) noisy keyboard c) +5v supply low	a) VG/GT card b) keyboard replacement c) adjust +5v
One cursor control fails to work	c) faulty keyboard	a) VG/GT card b) FE/GT card c) check cable, replace keyboard if faulty
REPEAT key fails to operate	b) faulty keyboard	a) FE/GT card b) check cable, replace keyboard if faulty
No cursor visible, but data on screen		a) VG/GT card b) MC/GT card
Cannot enter data	a) full duplex switch in FDX position b) modem off line but plugged into EIA connector c) faulty keyboard d) switch 2 on (FE/GT card)	a) switch to HDX (release switch) c) keyboard replacement d) turn switch off e) FE/GT card

Trouble	Probable Cause	Remedy or Bad Board
CR or ERASE fills rest of line or whole screen with some characters other than space		a) MC/GT card
Data from keyboard is entered in wrong lines sometimes		a) VG/GT card b) MC/GT card
Characters sometimes not entered on screen or missing from words		a) keying in too fast
Characters appear to be entered incorrectly in 1/3 of screen		a) MC/GT card
Characters appear to be entered incorrectly in all of screen		a) MC/GT card b) VG/GR card c) FE/GT card d) keyboard
Cursor Address function fails to operate		a) VG/GT card
Cursor Address operates but cursor goes to wrong location		a) VG/GT card
Line Address function fails to operate		a) VG/GT card
Line Address operates but cursor goes to wrong line		a) VG/GT card
Carriage Return fails to operate properly		a) MC/GT card b) FE/GT card
Characters don't scroll up screen		a) MC/GT card
Once data scrolls it doesn't stop; keeps scrolling		a) MC/GT card

Trouble	Probable Cause	Remedy or Bad Board
Data changes when shifting from bottom 1/3 to middle third or from middle third to top third of screen		a) MC/GT card
Printer fails to operate - power button seems to be ON	a) Power-ON indicator will show "ON" even though Printer is not plugged into AC outlet. Check by pushing LF button b) Not in PRINT ON mode c) not plugged into terminal d) faulty printer	a) plug in and check printer b) press PRINT ON c) plug into terminal d) replace printer
Characters to Printer not the same as on screen		a) FE/GT card b) bad printer
Printer fails to CR after printing only one character on a line when new line sent from terminal	a) printer out of adjustment	a) refer to Printer Manual
Printer returns to next line before the terminal has finished sending a given line	a) printer out of adjustment	a) refer to Printer Manual
EIA output data doesn't operate	a) bad cable b) wrong baud rate	a) repair cable b) correct setting c) FE/GT card d) "Clear to Send" false
EIA data input doesn't operate but output operates	a) cable wrong b) wrong baud rate	a) replace cable b) correct setting c) FE/GT card

Trouble	Probable Cause	Remedy or Bad Board
EIA interface operates but current loop doesn't	a) cable wrong b) wrong baud rate c) S2 on FE/GT d) loop polarities reversed	a) replace b) correct setting c) FE/GT card S2 on d) reverse polarity
Data to EIA device or from EIA device has high error rate but EIA device check OK	a) baud rate wrong b) frequency of baud rate incorrect	a) correct setting b) replace FE/GT card or adjust frequency
Terminal is hung up and one can't enter anything on screen	a) EIA cable plugged in with no device attached or power off	a) unplug cables
CARRIER light fails to come on but EIA appears to function	a) lamp bad b) EIA cable wrong c) FE/GT card	a) replace lamp b) check Carrier Detect signal c) replace FE/GT
"*" written on screen	a) parity error b) framing error	a) set switches on FE/GT card as per schematic b) check EIA device

7. POWER SUPPLY SUBASSEMBLY

This section describes the power supply used in the ADDS Consul series of desktop terminals and the MRD series of rack-mountable equipment. Except for minor variations, the same power supply is used in all Consul and MRD units.

The variations are:

a) Power Transformer - The type of transformer used in the power supply depends on whether the supply is to be installed in a Consul or an MRD.

b) Fan Placement - An exhaust fan is mounted integrally in power supply subassemblies used in Consul terminals. For MRD equipment the exhaust fan is not on the power supply subassembly but is mounted on the rear panel of the MRD instead.

7.1 Power Supply Specifications

7.1.1 Input Voltage

105-125 VAC/210-250 VAC (strapping option)

7.1.2 Input Frequency

47-63, 400 Hz

7.1.3 Input Breakout

Below 100/195 VAC

7.1.4 Outputs

(a)	+5.2 VDC ±10%	@	6.75 A continuous
(b)	+13.2 VDC	@	0.5 A continuous
(c)	-13.2 VDC	@	1.0 A continuous

7.1.5 Regulation

Line: ±0.5% Low Line to High Line for both 115V and 230 VAC

Load: ±0.5% No Load to Full Load

7.1.6 Ripple

10 mV RMS max.
30 mV Peak to Peak max.

7.1.7 Overload Protection

All outputs protected by individual foldback circuits against continuous overloads and short circuits. Automatic recovery upon removal of overload condition.

7.1.8 Overvoltage Protection

Individual crowbars for each output: +5.2 VDC output to be preset between +6.50 and +7.5 VDC.
The +13.2 VDC and -13.2 VDC outputs will be preset between 15.0 and 17.0 VDC.

7.1.9 DC Output Adjust

The 5.2 VDC output is settable by means of a Cermet potentiometer to ±10% of nominal. The +13.2 VDC and -13.2 VDC outputs are set by fixed resistors to ± 2% of nominal.

7.1.10 Temperature Coefficient and Stability

T.C.: 0.02%/°C
Stability: 0.1% for any 8 hour period after 30 min. stabilization.

7.1.11 Operating Temperature

-20°C to +55°C

7.1.12 Storage Temperature

-55°C to +85°C

7.1.13 Overtemperature Protection

Thermostat protection provided to turn off AC input in the event ambient temperature goes beyond 75°C. Heatsink temperature protected at 100°C to 108°C.

7.1.14 Fusing

To protect the power supply from internal faults an input fuse should be used. For 115V input a 1.5 A Slo-Blow fuse is recommended. A 0.75 A Slo-Blow fuse must be used for 230V input.

7.1.15 P.C. Boards

P.C. boards should be easily field replaceable without desoldering.

7.1.16 Humidity

The operating range is 0-95% R.H., non-condensing .

7.2 Theory of Operation

7.2.1 General Power Supply Description

The power supply consists of three separate series regulators obtaining their power from a common transformer. All three regulators are basically the same in design and operation. Only the sensing, drive and series-pass circuit vary slightly. Each circuit has a full wave rectifier, filter capacitor, complete IC regulator, pass transistor, driver and overvoltage SCR crowbar.

Fold out the power supply schematic drawing, Figure 7.5 on pages 7-17/18 before proceeding to the circuit description below.

7.2.2 Circuit Description

7.2.2.1 Input Transformer

Input voltage of 115 or 230 VAC is applied to transformer T1; see schematic for proper jumper connection on transformer for 115 or 230 VAC operation. All input and output connections are made through terminal board TB1.

7.2.2.2 5 Volt Regulator Circuit

The center tapped transformer winding feeds rectifiers CR2 and CR3 and the rectified DC is filtered by capacitor C6. The filtered unregulated DC is then fed to the collector of series-pass transistors Q4, Q5 which produce the proper voltage drop to keep the output regulated at the preset voltage. IC regulator A1 consists of voltage reference, error amplifier series-pass transistor and current limit circuit. The output voltage is connected directly to the inverting input. The reference voltage is connected to a voltage divider R7, R8 and R9. The reference voltage is divided down to 5 V with potentiometer R8 and fed to the non-inverting input. The regulator will then automatically adjust and maintain the output voltage at the voltage set with potentiometer R8. R8 allows to vary the output voltage at least ±10%. The output of the IC regulator feeds driver Q1 which controls passing transistors Q4 and Q5. Overload protection is provided by sensing the voltage drop across emitter resistor R18, R19 plus base-emitter voltage of Q4 and Q5. The sense voltage is picked up through voltage divider R5, R6 and is fed to the

IC regulator in such a manner that drive to Q1 is removed in case excessive current is drawn. In case of a short circuit only a fraction of the nominal output current can be drawn. The input to A1 is fed from the +13.2 V output, because the IC regulator requires a voltage several volts greater than its output. Therefore, the +5 V circuit depends on the presence of the +13.2 V output.

7.2.2.3 <u>+13 and -13 V Regulator Circuit</u>

Both circuits are identical except for the pass transistor drive circuits. The transformer secondary winding feeds rectifiers CR6 and CR7 and the rectified DC is filtered by capacitor C7. The filtered, unregulated DC is then fed to the collector of series-pass transistor Q6 which produces the proper voltage drop to keep the output regulated at the preset voltage.

Except for the sensing bridge, the 13V circuits operate exactly like the 5V circuit described above. The reference voltage from pin 4 of IC A1 is fed directly ot the non-inverting input pin 3. R9, 10 and 11 is a voltage divider, dividing the output voltage down to same level as the reference voltage (approx. 7.15V) This sample of the output voltage is then fed to the inverting input pin 2. Jumpers J2 and J3 across R11 are used to set the output voltage to within ±2%. The -13.2 output has its own recitifer-filter circuit (CR10-CR13, C8) The positive output terminal is connected to the output common.

7.2.2.4 <u>Overvoltage Crowbar Circuit</u>

Silicon controlled rectifiers Q8, Q9 and Q10 are connected across the outputs of each of the three regulators. Zener diode VR2, R14, R15 and R17 form a sensing bridge to detect an overvoltage. Q2 is normally not conducting. In case of an overvoltage Q2 will turn on and fire the SCR which causes the output voltage to drop. All three overvoltage circuits work in the same fashion.

7.3 Operating Notes

Connections to the power supply are made through the appropriate terminals on the terminal board. The output voltages are factory pre-set. (The +5V output can be adjusted with potentiometer R8.) The power supplies are designed to operate with forced air. Should the fan fail or airflow be severely restricted, the heatsink will get excessively hot and the thermostat K1 will open, interrupting input power. Operation will continue after the power supply has sufficiently cooled off. If this should occur, operation should be discontinued until proper air flow is restored.

Similarly, a short in the terminal backplace wiring could cause the power supply to shut down. If this is suspected disconnect the output leads (+5.2 VDC, +13 VDC, -13 VDC) from the barrier strip on the power supply and observe whether or not the output voltages at the barrier strip come up to the correct value with the harness to the terminal electronics disconnected. If so, there is a short in the terminal backplane (or P.C. cards) rather than a fault in the power supply itself.

7.4 Maintenance

7.4.1 General

This section describes trouble analysis routines and test procedures that are useful for servicing the power supply. A chart is provided for trouble shooting. Refer to section 7.1 for minimum performance standards.

7.4.2 Trouble Analysis Procedures

Whenever a problem develops, systematically check all fuses, primary power connections, external circuit elements, and external wiring before trouble shooting the equipment. Failures and malfunctions often can be traced to simple causes such as improper jumpers and supply load connections or fuse failure. Use the schematic diagram as an aid to locating trouble causes. The voltage chart contains various circuit voltages that are averages for normal no-load operation. Use measuring probes carefully to avoid causing short circuits and damaging circuit components.

7.4.3 Checking Transistors and Capacitors

Check transistors with an in-circuit transistor checker. If no checker is available, transistors can be checked with an ohm-meter that has a highly limited current capability. Observe proper polarity for NPN transistors. The forward transistor resistance is low but never zero; backward resistance is always much higher than the forward resistance.

When soldering semi-conductor devices, hold the lead being soldered with pliers on a heat sinking device placed between the component and the solder joint.

Note: The leakage resistance obtained from a simple resistance check of a capacitor is not always an indication of a faulty capacitor. In most cases the capacitors are shunted with resistances some of which have low values. Only a dead short is a true indication of a shorted capacitor.

7.4.4 Printed Circuit Board Maintenance Techniques

Voltage measurements can usually be made from both sides of the board. Use a needle point probe or another suitable measuring probe.

Broken or damaged printed wiring is usually the result of an imperfection or strain. To repair small breaks, tin a short piece of hook-up wire to bridge the break and holding the wire in place, flow solder along the length of wire so that is becomes a part of the circuit.

When unsoldering components from the board never pry or force the part loose, use a solder-sucker to remove solder before loosening a component. If a solder-sucker is not available, use tinned copper braid or stranded wire (AWG 14 or 16).

7.4.5 Trouble Chart Description

The trouble chart is intended as a guide for locating trouble causes, and is used along with the schematic.

The operating conditions assumed for the trouble chart are as follows:

(a) AC power of proper voltage and frequency is present at the input terminals.

(b) All loads have been removed.

7.4.6 Typical Voltages

Voltage readings taken at nominal AC line voltage and no load.

T1	7-12	18.5 VAC
	5-6, 5-11	10.4 VAC
	8-13	19.2 VAC
C6		14.3 VDC
C7		24.5 VDC
C8		26.2 VDC
C1		-
Com. output -	PC1/A1-4	6.8- 7.5 VDC
" "	PC2/A1-4	6.8 -7.5 VDC
-13V output -	PC3/A1-4	6.8 -7.5 VDC
	PC1/VR2	3.3 VDC
	PC2/VR2	5.6 VDC
	PC3/VR2	5.6 VDC
Com. output -	PC1/Q1 base	6.35VDC
" " -	PC2/Q1 base	14.45VDC
-13V output -	Q7 base	13.8 VDC
Com. output -	Q4 base	5.6 VDC
" "	Q6 base	13.8 VDC

7.4.7 Trouble Chart

Symptoms	Probable Cause	Remedy
1. No output voltage	K1 open	Replace K1 if it does not reset when cool.
	T1 defective	Check T1 for proper output voltage; replace.
	A1 defective	Replace if no output on pin 6 or no reference voltage on pin 4.
2. Low Output Voltage	Q1 open	Check & Replace.
	Q4,5 Q6 Q7 open	Check & Replace.
	CR2,3 CR6,7 (8,9) } defective CR10-13	Check & Replace.
	C4 shorted	Check & Replace.
	SCR fired	Raise input voltage slowly and check if OV ckt. crowbars at the right voltage. If yes, check output too high. Check for shorted SCR.
3. Output Voltage too High. Note: High output may activate OV-circuit	Q4,5, Q6,Q7 shorted	Check & Replace.
	A1 defective.	Check & Replace.
4. High Ripple & Unregulated DC.	AC input voltage too low.	Check AC line voltage.
	Open Rectifier CR2-13	Check & Replace.
	Excessive Load.	Check Load Current.

Notes:

(a) The +5 Volt output depends on +13 Volt. Check +13V output before trouble shooting +5V output.

(b) High output may activate OV. crowbar. Trouble shoot with reduced input voltage. (Use variable transformer to keep output voltage below trip voltage.)

(c) If trouble is suspected to be on PC board, replace entire board if one is available.

7.4.8 Power Supply Drawings/Photographs

Presented on following pages are:

Figure 7.1 - A photo of the Consul power supply.

Figure 7.2 - A photo of the MRD power supply.

Figure 7.3 - Photos of the three P.C. boards on the power supply.

Figure 7.4 - Diagram of harness connection to power supply barrier strip.

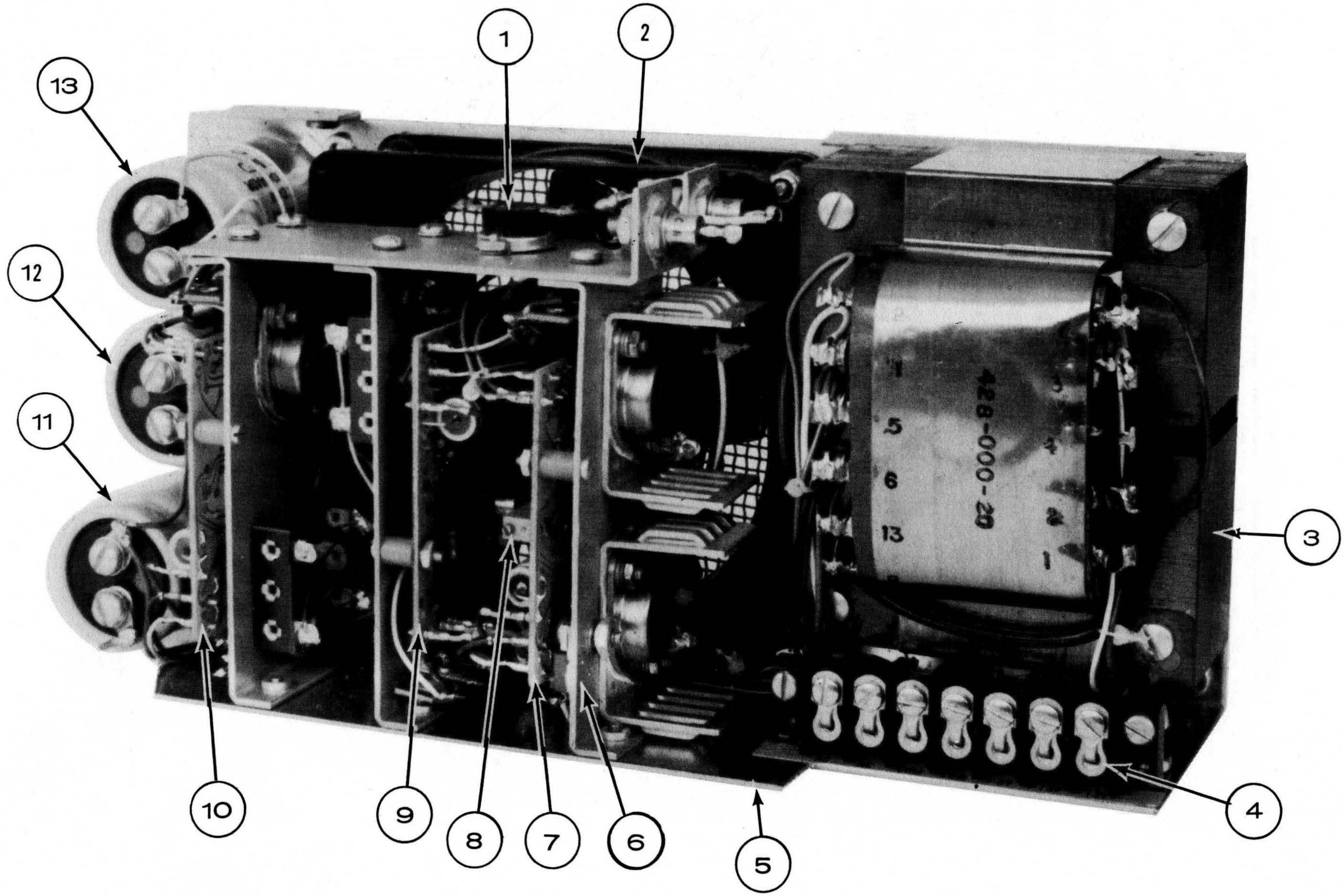
Figure 7.5 - Power Supply schematic drawings.

In Figures 7.1 and 7.2, the major components identified are as follows:

1. Thermostat
2. Fan
3. Power transformer (T1)
4. Terminal board (TB1)
5. Chassis
6. Heat sink bracket
7. +5 VDC P.C. Board (PC1)
8. Potentiometer (+5V adj)
9. -13.2 VDC P.C. Board (PC3)
10. +13.2 VDC P.C. Board (PC2)
11. Filter capacitor (C6)
12. Filter capacitor (C7)
13. Filter capacitor (C8)

CONSUL SERIES POWER SUPPLY, 285·002

Fig. 7·1



MRD SERIES POWER SUPPLY, 285-004

Fig. 7-2

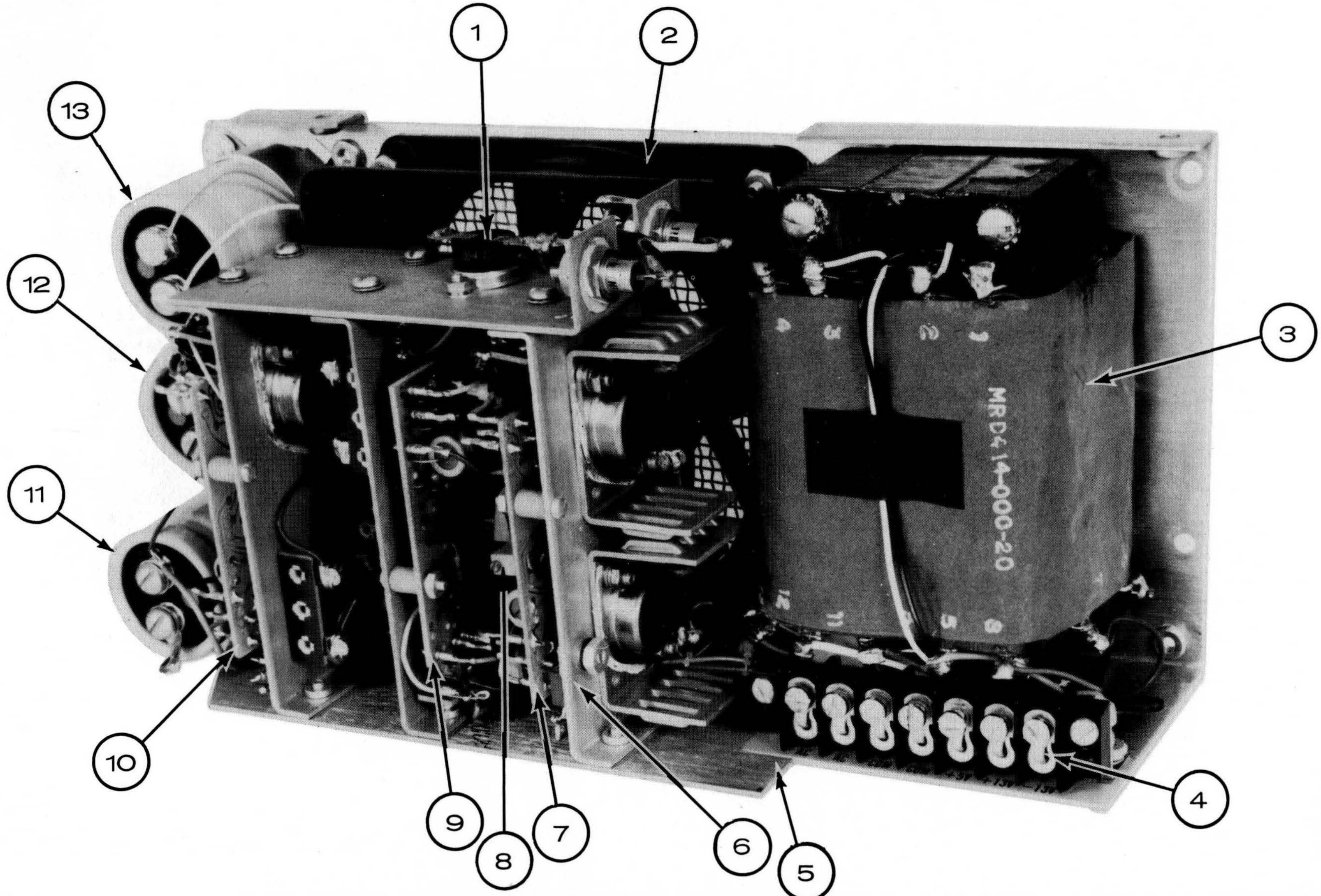
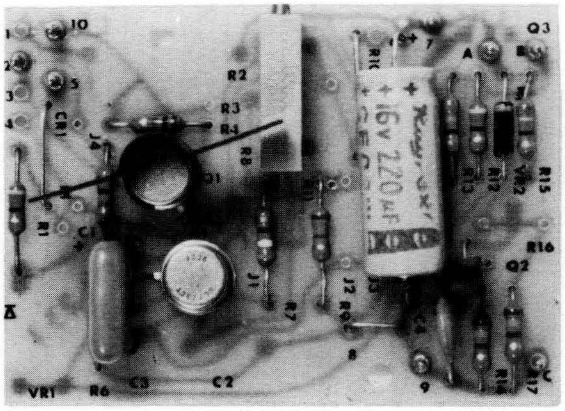
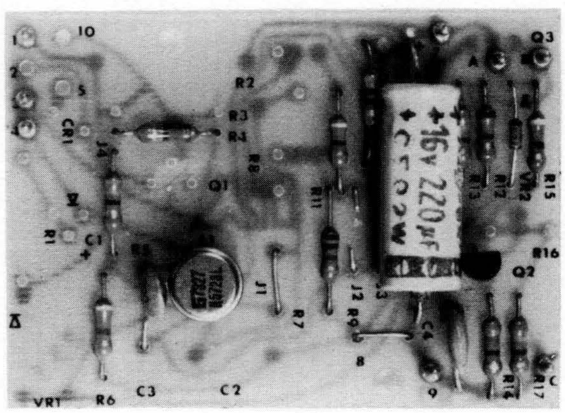


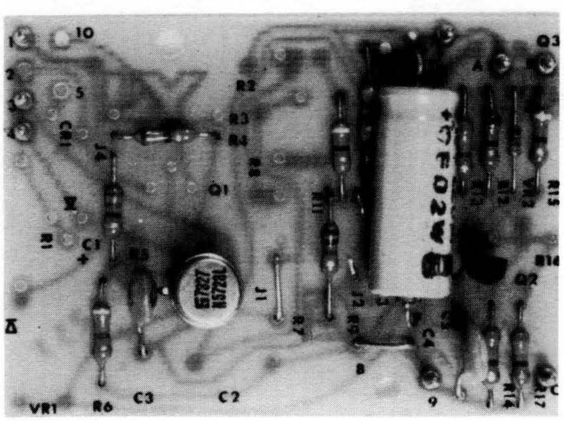
Fig. 7·3



+5VDC · PC1 · 360·110



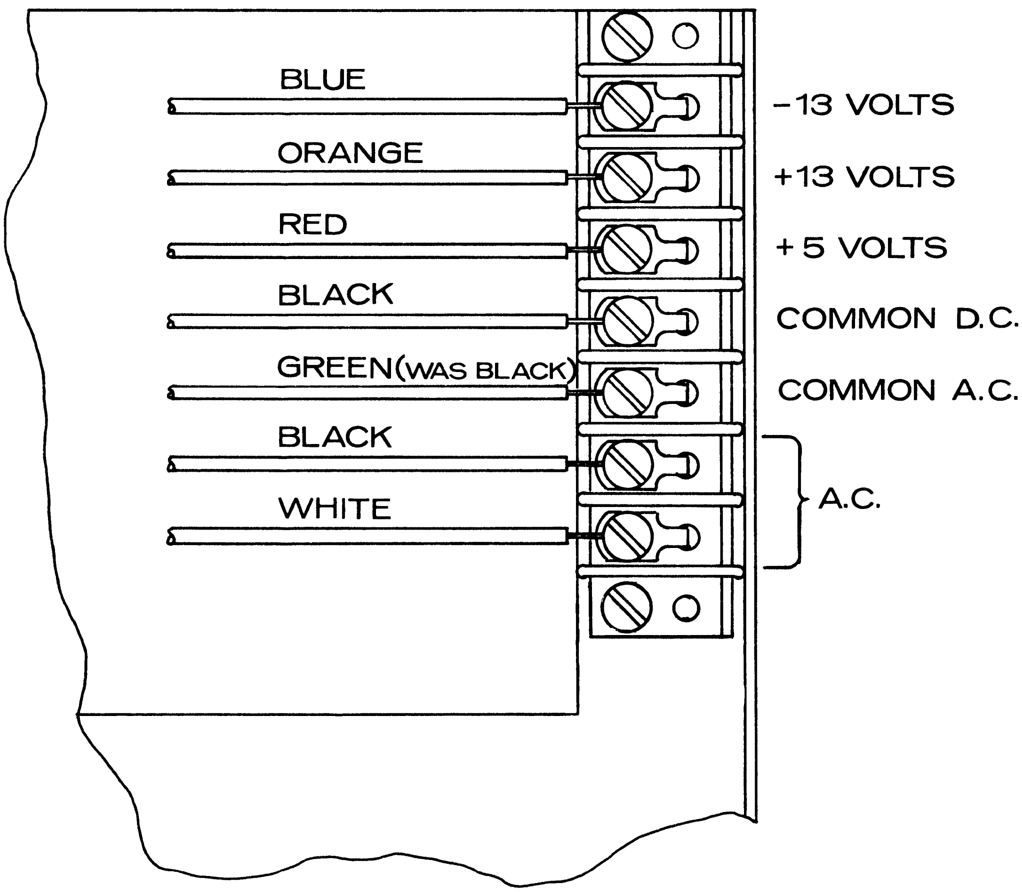
+13.2VDC · PC2 · 360·132



−13.2VDC · PC3 · 360·115

POWER SUPPLY TBI CABLE HOOK-UP

Fig. 7·4



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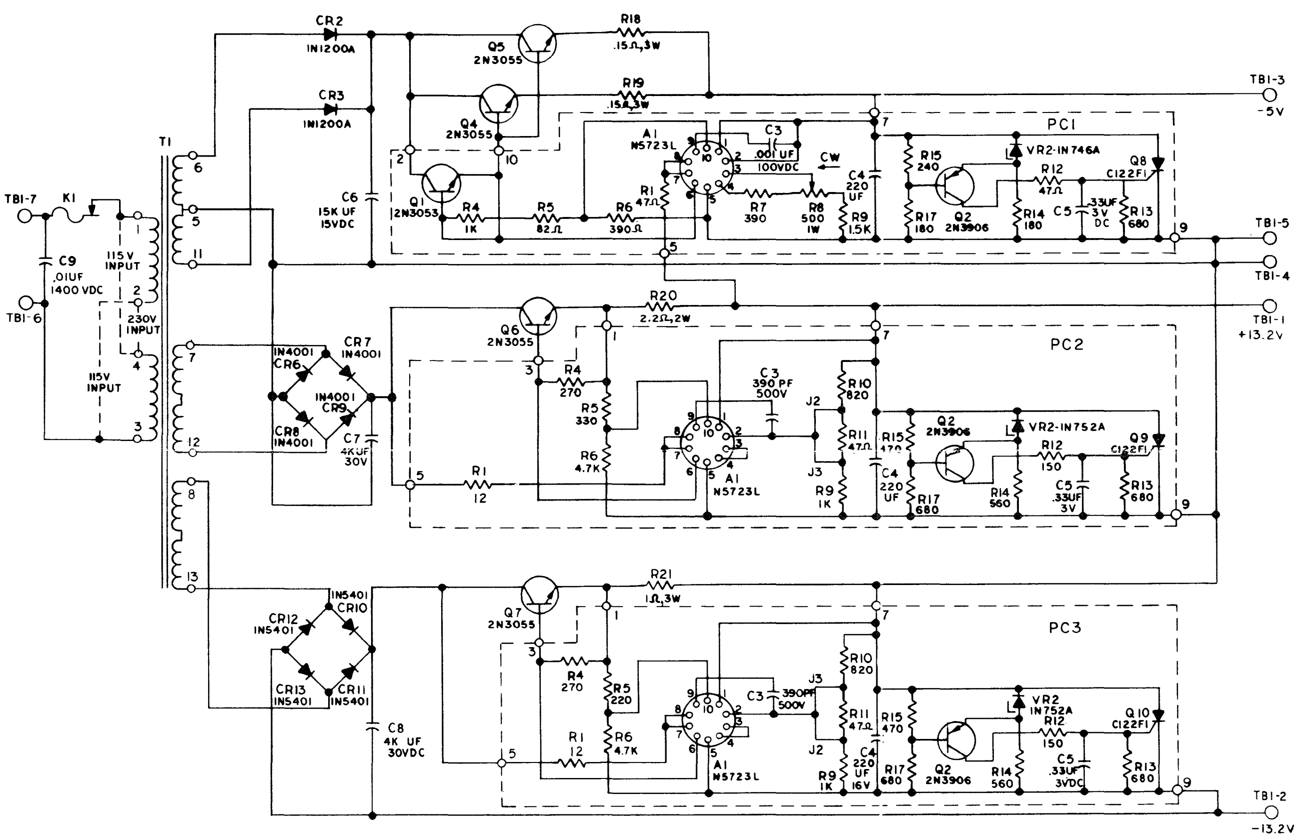
REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	ADDED R1		



NOTE
UNLESS OTHERWISE SPECIFIED
RESISTORS ARE 1/4 W, 5%

Figure 7.5

	580	1
	800A	1
	880	1
NEXT ASSY	USED ON	QTY

TOLERANCES 1/64 .005 1° FRAC DEC ANG
DO NOT SCALE DWG

ADDS Applied Digital Data Systems, Inc. Hauppauge, New York

SCHEMATIC DIAGRAM
POWER SUPPLY

DWG NO 285-002 SIZE D REV A

7.5 Power Supply Bill of Material

A complete B.O.M. of the Power Supply is given in following pages.

Note that for certain parts, ADDS is the sole supplier. However most parts are "off the shelf" and have a standard manufacturer's part number listed.

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	502-010A	1	ASS'Y. POWER SUPPLY		
2	285-002	1	POWER SUPPLY ASSEMBLY	POWER PAC 417-000-91	
3	502-003B	1	ASS'Y. PLENUM		
4	502-714C	1	COVER, POWER SUPPLY		
5	502-733A		SCREEN, FAN		
6	825-003	1	FAN	IMC-WS2107FL-2R	
7	810-005	11	6-32 x 5/16 SCREW	SEMS	
8	746-008-S-1	4	6-32 x 1/2 SCREW, P.H. PHILLIPS, CRS CAD PLATE		
9	790-008-S-1	2	6-32 FLAT WASHER, CRS, CAD PLATE		
10	360-089	AR	CATERPILLAR INSULATOR TRACK		
11	360-023	1	CABLE CLAMP	WECKESSER #5/32J	

PREPARED	P.George	11-7-73	TITLE ASS'Y. POWER SUPPLY	
CHECKED			DWG. NO. 502-010	REV. A
APPROVED			SHEET 2 OF 2	

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	285-002	1	TOP ASSY. POWER SUPPLY +5.0 VDC ADJUSTABLE,	POWER PAC 417-000-91	
			+13.2 VDC AND -13.2 VDC		
2		1	MAIN CHASSIS		
3	360-110	1	P.C. BOARD +5.0V	ADDS	PC-1
4	360-115	1	P.C. BOARD -13.2V	ADDS	PC-2
5	360-132	1	P.C. BOARD +13.2V	ADDS	PC-3

PREPARED			TITLE TOP ASSY - POWER SUPPLY		
CHECKED			DWG. NO. 285-002	REV. A	SHEET 1 OF 5
APPROVED					

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	CHASSIS		
2		2	BRACKET-P.C. BOARD		
3		1	BRACKET-P.C. BOARD		
4		1	BRACKET RECTIFIER		
5		2	HEAT SINK - T03	STAVER 65	
6		3	TERMINAL STRIP	CINCH-JONES 52A	
7		4	TERMINAL STRIP	CINCH-JONES 52	
8		3	CAPACITOR CLAMP	SPRAGUE 4586-97A	
9		1	TERMINAL BLOCK	CINCH-JONES 7-140Y	TB1-1
10	350-008	1	TRANSFORMER	ADDS	T1
11		2	RIGHT ANGLE BKT'S	H.H. SMITH 1446	
12		6	FIBER STANDOFF	H.H. SMITH 8886	
13	140-087	1	ELECT. CAP 15K uf, 15 VDC	SPRAGUE 36DX153G015AB2	C6
14	140-088	2	ELECT. CAP 4K uf, 30 VDC	SPRAGUE 36DX402G030AA2	C7,C8
15		2	RECTIFIER-STUD MOUNT	INT. RECT. CORP. 1N1200A	CR2,CR3
16		4	RECTIFIER-AXIAL LEAD	PWR. COMP. 1N4001	CR6 thru CR9
17		4	RECTIFIER-AXIAL LEAD	PWR. COMP. 1N5401	CR10 thru CR13
18		1	THERMOSTAT	KLIXON 20700	K1
19	330-010	4	TRANSISTORS-T03	MOTOROLA 2N3055	Q4 thru Q10
20		1	CAPACITOR-AC .01 uf, 1400 VDC	DIELECTRON ULR1400DC	C9
21		3	SCR	G.E. C122F1	Q8 thru Q10
22		2	RESISTOR W.W. .15ohm 3W	CLAROSTAT CC3L	R18,R19
23		1	RESISTOR W.W. 2.2 ohm 2W	IRC BWH	R20
24		1	RESISTOR W.W. 1.0 ohm 3W	CLAROSTAT CC3L	R21
25		1	MARKING STRIP-VOLTAGE DESIGNATION		
26					

PREPARED	I.C. Serra	11/3/73	TITLE MAIN CHASSIS - POWER SUPPLY	ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. / REV. A / SHEET 2 OF 5	
APPROVED				

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	360-110	1	PRINTED CIRCUIT BOARD, +5 V	ADDS	PC-1
2		1	CAPACITOR .001 uf 100VDC	SPRAGUE 225	C3
3		1	CAPACITOR 220 uf 16VDC	RAYREX RADY 220 PY01605	C4
4		1	CAPACITOR .33 uf 3VDC	DIELECTRON RT3	C5
5		1	RESISTOR 47 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R1
6		1	RESISTOR 1K ohm 1/4W ± 5%	ALLEN BRADLEY EB	R4
7		1	RESISTOR 82 ohm 1/4W ± 5%	ALLEN BRADLEY EB	R5
8		1	RESISTOR 390 ohm 1/4W ± 5%	ALLEN BRADLEY EB	R6
9		1	RESISTOR 47 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R12
10		1	RESISTOR 680 ohm 1/4W ± 5%	ALLEN BRADLEY EB	R13
11		1	RESISTOR 180 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R14
12		1	RESISTOR 390 ohm 1/4 W	R-OHM R-25	R7
13		1	RESISTOR 270 ohm 1/4 W	R-OHM R-25	R15
14		1	RESISTOR 180 ohm 1/4 W	R-OHM R-25	R17
15		1	RESISTOR 1.5K ohm 1/4W	R-OHM R-25	R9
16		1	POT 500 ohm 1 W	AMPHENOL 6034P-501-7310	R8
17	330-018	1	TRANSISTOR TO-5	RCA 2N3053	Q1
18	330-005	1	TRANSISTOR TO-92	NATIONAL 2N3906	Q2
19		1	ZENER DIODE	MOTOROLA 1N746A	VR2
20		1	REGULATOR	SIGNETICS N5723L	A1
21		1	TO-5 HEAT SINK	WAKEFIELD 296-1-AB	

PREPARED	I.C. Serra	11/3/73	TITLE CONSUL POWER SUPPLY	
CHECKED			DWG. NO. 360-110	REV. A
APPROVED			SHEET 3 OF 5	

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	360-110	1	PRINTED CIRCUIT BOARD, +13.2 V	ADDS	PC-2
2		1	CAPACITOR 390 pf 500V	DIELECTRON X5F	C-3
3		1	CAPACITOR 220 uf 16V	RAYREX RADY 220PY01605	C-4
4		1	CAPACITOR .33 uf 3 Volt	DIELECTRON RT3	C5
5		1	RESISTOR 270 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R4
6		1	RESISTOR 47 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R11
7		1	RESISTOR 150 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R12
8		1	RESISTOR 680 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R13
9		1	RESISTOR 560 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R14
10		1	RESISTOR 4.7K ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R6
11		1	RESISTOR 330 ohm 1/4 W	R-OHM R-25	R5
12		1	RESISTOR 1.K ohm 1/4 W	R-OHM R-25	R9
13		1	RESISTOR 470 ohm 1/4 W	R-OHM R-25	R15
14		1	RESISTOR 680 ohm 1/4 W	R-OHM R-25	R17
15		1	RESISTOR 820 ohm 1/4 W	R-OHM R-25	R10
16		1	ZENER DIODE	MOTOROLA 1N752A	VR2
17		1	REGULATOR	SIGNETICS N5723L	A1
18		1	TRANSISTOR TO-92	NATIONAL 2N3906	Q2

PREPARED	I.C. SERRA	11/3/73	TITLE CONSUL-POWER SUPPLY		ADDS Applied Digital Data System, Inc. Hauppauge, New York
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BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	360-110	1	PRINTED CIRCUIT BOARD -13.2 V	ADDS	PC-3
2		1	CAPACITOR 390 pf, 500VDC	DIELECTRON X5F	C3
3		1	CAPACITOR 250 uf, 16 VDC	RAYREX-RADY 220PY01605	C4
4		1	CAPACITOR .33 uf, 30 VDC	DIELECTRON RT3	C5
5		1	RESISTOR 270 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R4
6		1	RESISTOR 4.7K ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R6
7		1	RESISTOR 47 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R11
8		1	RESISTOR 150 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R12
9		1	RESISTOR 680 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R13
10		1	RESISTOR 560 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R14
11		1	RESISTOR 220 ohm 1/4 W	R-OHM R-25	R5
12		1	RESISTOR 1K ohm 1/4 W	R-OHM R-25	R9
13		1	RESISTOR 820 ohm 1/4 W	R-OHM R-25	R10
14		1	RESISTOR 470 ohm 1/4 W	R-OHM R-25	R15
15		1	RESISTOR 680 ohm 1/4 W	R-OHM R-25	R17
16		1	TRANSISTOR TO-92	NATIONAL 2N3906	Q2
17		1	ZENER DIODE	MOTOROLA 1N752A	VR2
18		1	REGULATOR	SIGNETIC N5723L	A1

PREPARED	I.C. Serra	11/3/73	TITLE CONSUL POWER SUPPLY	
CHECKED			DWG. NO. 360-115	REV. A
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BILL OF MATERIAL

8. TV MONITOR SUBASSEMBLY

8.1 General Description

The TV monitor is a solid-state unit intended for use in industrial and commercial installations where reliability and high quality video reproduction are desired. It is packaged as a self-contained subassembly, complete with a power supply. The only electrical connections required to the monitor subassembly are AC power and horizontal and vertical video drive signals.

The monitor subassembly can easily be removed from your terminal by removing three nuts which hold the unit on mounting studs and disconnecting the 10-pin edge connector and the AC power "Molex" connector. Note that re-centering the picture may be necessary when installing a new monitor. See Section 8.4.4 for details.

8.2 Specifications

8.2.1 Input Data Specifications

	Video	Vertical Drive Signal	Horizontal Drive Signal
Input Connector	(Necessary Accessory-Available) Printed circuit board card edge connector - Viking #2VK10S/1-2 or Amphenol #225-21031-101		
Pulse Rate or Width	Pulse Width: 100 nsec or greater	Pulse Rate: 47 to 63 pulses per second	Pulse Rate: 15,000 to 16,500 pulses per sec
Amplitude	Low = Zero $^{+0.4}_{-0.0}$ volts High = 4 $\pm$ 1.5 volts		
Signal Rise & Fall Times (10% to 90% amplitude)	Less than 20 nsec	Less than 100 nsec	Less than 50 nsec
Input Signal Format	See Figure 8.1		

8.2.2 Display Specifications

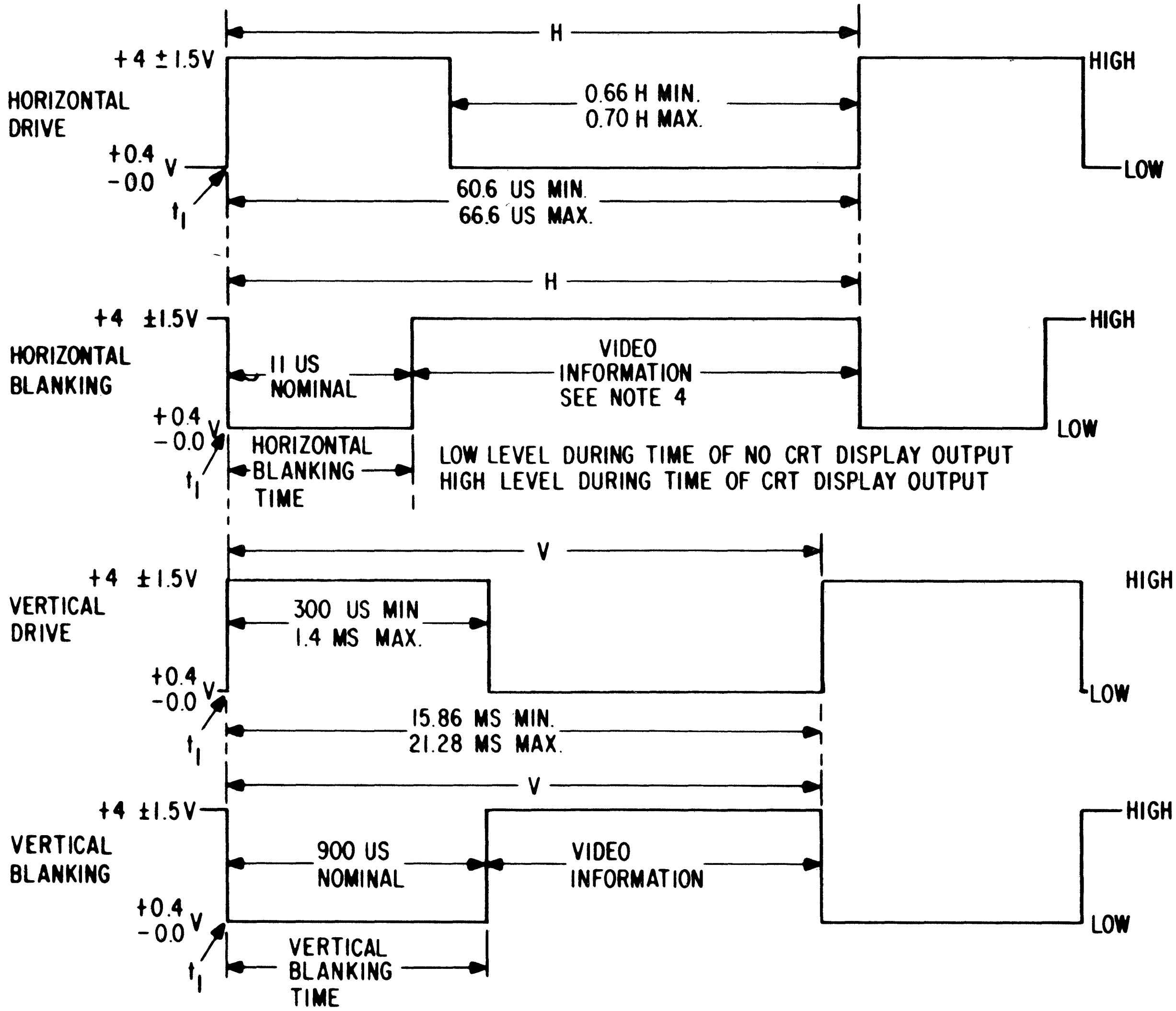
(a) Cathode Ray Tube

Nominal Diagnal Measurement: 12 inches

Phosphor: P4

SYNCHRONIZATION AND BLANKING SIGNALS

Fig 8.1



NOTES

1. The leading edges of Drive and Blanking waveforms must start at time t_1. Nominal Blanking times should be observed.
2. H = time from start of one line to start of next line.
3. V = time from start of one field to start of next field.
4. Video pulse width should be equal to or greater than 100 nsec.

*Resolution (TV Lines): at center - 900 at 40 fL
at corner - 800 at 40 fL

*Resolution is measured in accordance with EIA RS-375, except Burst Modulation (or Depth of Modulation) is adjusted for 100 percent.

b) Geometric Distortion

The perimeter of a full field of characters shall approach an ideal rectangle to within ±1.5% of the rectangle height.

8.2.3 Power Requirements

Input Connector:	Receptacle, Molex #03-06-1041 supplied with unit. Mating plug is Molex #03-06-2041.
Input Voltage:	105 to 130 V rms (120V nominal; 50/60 HZ) Optional: 220/240 V rms ± 10%; 50/60 HZ.
Input Power:	24 Watts (nominal)
Output Voltages:	+15VDC (short circuit protected) +12 kV DC;

8.2.4 Environmental Specifications

a) Temperature

Operating Range: 5°C to 55°C
Storage Range: -40°C to 65°C

b) Humidity

5 to 80 percent R.H. (noncondensing)

c) Altitude

Operating Range: Up to 10,000 feet

8.2.5 X - Ray Radiation

These units comply with DHEW Rules-42-CFR-Part 78.

8.2.6 Controls

a) External Controls

(1) Contrast, 500 ohm potentiometer carbon composition $\geq$1/4 Watt.

(2) Brightness, 100 kilohm potentiometer $\geq$1/4 Watt.

b) Internal Set Up Controls

(1) Height

(2) Vertical Linearity

(3) Vertical Hold

(4) Focus

(5) Width

(6) Low Voltage Adjust

8.3 Theory of Operation

Fold out the monitor schematic drawing, Figure 8.2, before proceeding with the theory of operations. Figure 8.2 is located at the end of this section, on page 8-11.

8.3.1 Video Amplifier

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101, operating as a class B amplifier, and its components comprise the video output driver with a gain of about 17.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

8.3.2 Vertical Deflection

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable resistor R116 and capacitors C105 and C106 form an RC network providing proper timing.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113.

The sawtooth voltage at the anode of Q102 is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and therby maintains excellent impedance isolation between Q102 and Q104. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power transistor which operates as a class A amplifier. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relative high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscilations by providing damping across the vertical deflection coils.

8.3.3 Horizontal Deflection

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. A positive going pulse is coupled through R127 to the base of Q105.

The driver stage is either cut off or driven into saturaction by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q105 into cut off, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by C110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer-coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12kV, "C" VDC, and "B" VDC respectively. 12kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier, Q101.

8.3.4 Low Voltage Regulated Supply

The series-pass low voltage regulator is designed to maintain a constant DC output for changes in input voltage, load impedance and temperature. Also included is a current limiting circuit designed to protect transistors connected to the "A" VDC output of the regulated supply from accidental output short circuits and load malfunctions.

The low voltage regulator consists of Q201, Q202, Q1, VR201, and their components. Q203 and its circuitry control the current limiting feature.

The 120 VAC primary voltage (220/240V, optional) is stepped down at the secondary of T1 where it is rectified by a full wave bridge rectifier CR1. Capacitor C1 is used as a filter capacitor to smooth the rectified output of CR1. Transistor Q1 is used as a series regulator to drop the rectified voltage to "A" VAC and to provide a low output impedance and good regulation. Resistor network R207, R208 and R209 is used to divide down the "A" VDC voltage to approximately +6 VDC and apply this potential to the base of Q202. A reference voltage from zener diode VR201 is applied to the emitter of Q202. If the voltages applied to the base and emitter of Q202 are not in the proper relationship, an error current is generated through Q202. This error current develops a voltage across R202 which is applied to the base of emitter follower Q201 and then applied to the base of Q1 to bring the output voltage back to its proper level. R201 and C201 provide additional filtering of the rectified DC voltage.

The short circuit protection or current limiting action can be explained as follows. Assume the "A" VDC bus becomes shorted to ground. This reduced output voltage is sensed by the base of Q202 turning that transistor off because of the reverse bias across its emitter and base junction. Simultaneously, the increased current through R204 increases the forward voltage drop across the base and emitter junction of Q203 and turns it on. Prior to the short circuit condition, Q203 was cut off. The increased collector current through R202 decreases the collector voltage of Q203 which is detected by the base of Q201 and direct-coupled to the base of Q1 causing that conductor to conduct less. This closed loop operation maintains the current available to any transistor connected to the "A" VDC bus at a safe level during a short circuit condition.

8.4 Adjustments

8.4.1 Vertical Adjustments

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

(1) Set the vertical frequency control, R116, near the mechanical center of its rotation.

(2) Adjust the vertical height control, R124, for desired height.

(3) Adjust the vertical linearity control, R121, for best vertical linearity.

(4) Remove the vertical drive signal from the unit. Or, alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.

(5) Readjust the vertical frequency control, R116, until the picture rolls up slowly.

(6) Restore vertical drive to the monitor.

(7) Recheck height and linearity.

8.4.2 Horizontal Adjustments

Raster width is affected by a combination of the low voltage supply, width coil L101, and the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

(1) Adjust the horizontal width coil, L101, for the desired width.

(2) Adjust the linearity sleeve under the yoke to obtain the best linearity. Although this adjustment will affect the raster width,

it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.

(3) Readjust L101 for proper width.

(4) Observe final horizontal linearity and width, and touch up either adjustment if needed.

8.4.3 Focus Adjustment

The focus control, R107, provides an adjustment for maintaining best overall display focus.

8.4.4 Centering

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

The ring magnets should not be used to offset the raster from its nominal center position because it would degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

8.5 Troubleshooting and Maintenance

8.5.1 List of Symptoms and Remedy

SYMPTOM	POSSIBLE REMEDY
a) Screen is dark	If an external monitor is available, plug it into the video connector at the rear of the terminal. If no picture appears on that monitor check the P.C. cards in the terminal bucket which generate horizontal and vertical drive (The VGA and VGB in the 800/700 series; the VG/GT card in the 580/380 series)
	If external monitor shows picture (or if you cannot check P.C. cards in terminal) proceed to step below.
	Check "A" bus Q106, Q105, CR2

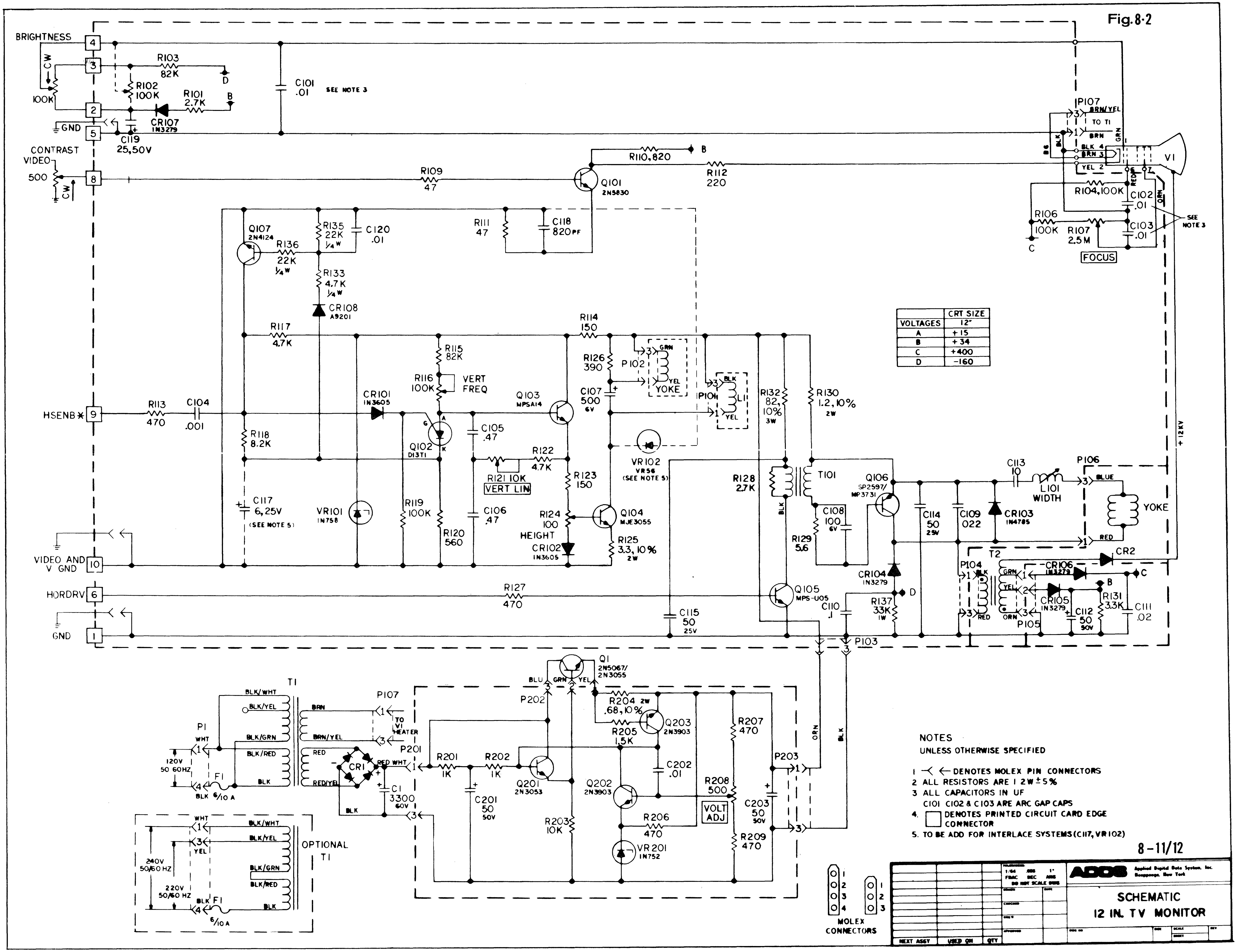
b)	Loss of Video	CR105, Q101
c)	Power consumption is too high	Check horizontal drive waveform; Check proper placement of horizontal linearity sleeve; Q106, Q105
d)	Low voltage bus incorrect	Q202, Q203, Q1 Note: Low voltage supply will indicate low or "0" volts due to its current limiting action if a short is evident in the "A" volt line.

8.5.2 Supplementary Drawings

The following four pages show

- A schematic drawing
- Interconnecting cabling
- Important waveforms in the monitor subassembly
- Location of Circuit Board Components

Fig. 8-2



VOLTAGES	CRT SIZE 12"
A	+15
B	+34
C	+400
D	-160

NOTES
UNLESS OTHERWISE SPECIFIED

1. —< ← DENOTES MOLEX PIN CONNECTORS
2. ALL RESISTORS ARE 1/2W ±5%
3. ALL CAPACITORS IN UF
   C101 C102 & C103 ARE ARC GAP CAPS
4. ☐ DENOTES PRINTED CIRCUIT CARD EDGE CONNECTOR
5. TO BE ADD FOR INTERLACE SYSTEMS (C117, VR102)

8-11/12

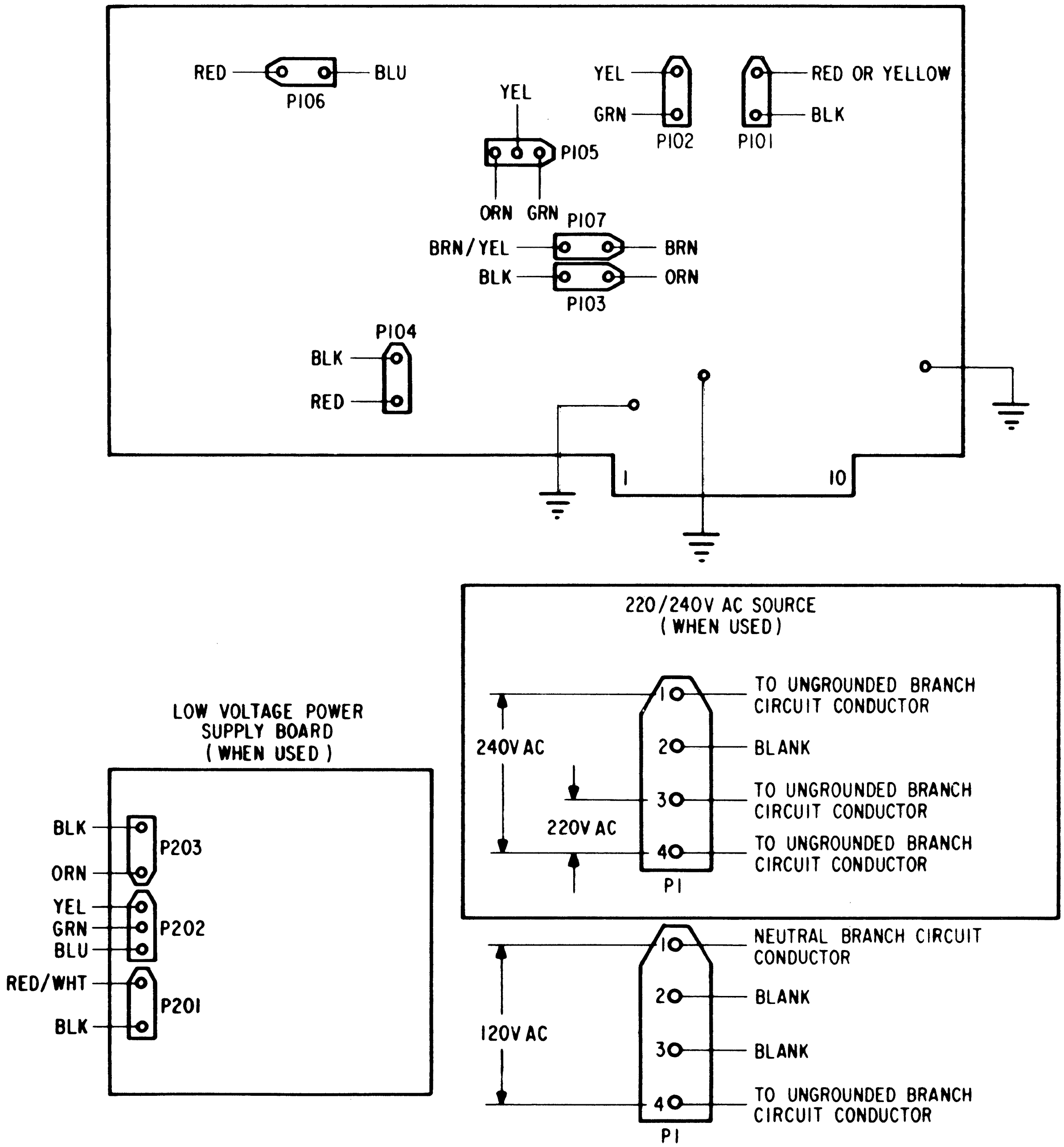
ADDS Applied Digital Data Systems, Inc. Hauppauge, New York

SCHEMATIC
12 IN. TV MONITOR

NEXT ASSY	USED ON	QTY

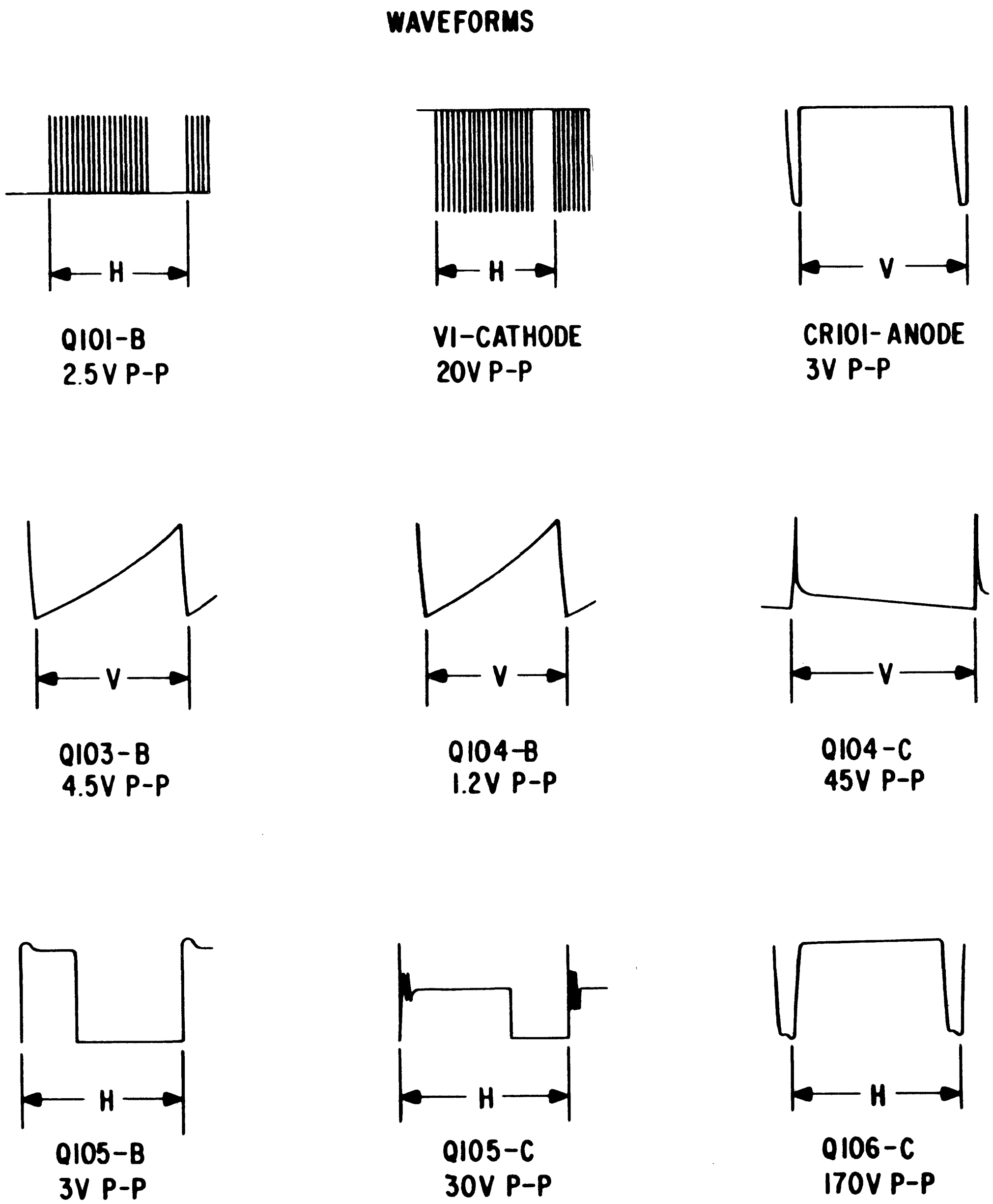
INTERCONNECTING CABLING

Fig. 8.3



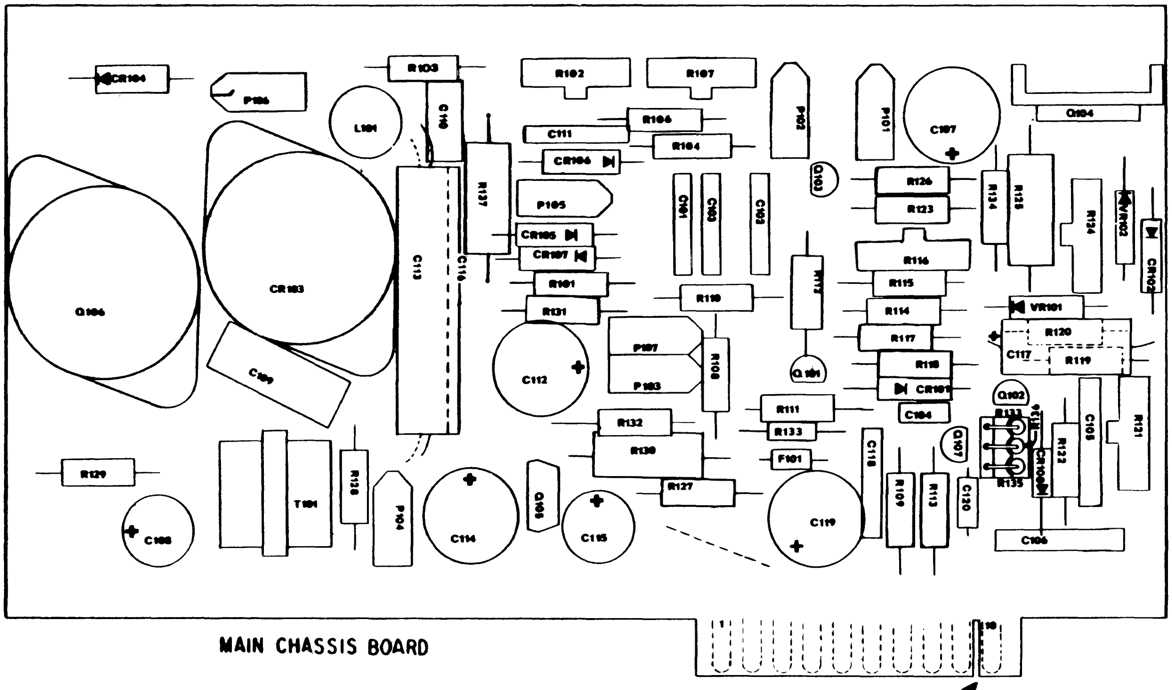
VOLTAGE WAVEFORMS

Fig. 8.4



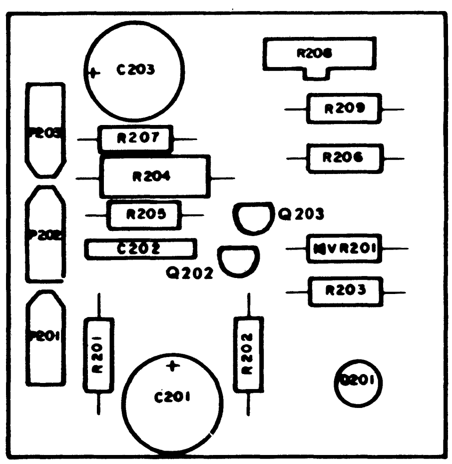
CIRCUIT BOARD COMPONENTS LOCATION

Fig.8.5



MAIN CHASSIS BOARD

KEYWAY FOR CONNECTOR POLARIZATION



LOW VOLTAGE POWER SUPPLY BOARD

8.6 TV Monitor Bill of Material

A complete B.O.M. of the TV Monitor is given in the following pages.

Note that for certain parts, ADDS is the sole supplier. However those parts which are "off the shelf" have a standard manufacturer's part number listed.

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	502-015A	1	ASS'Y., CRT		
2	502-713E	1	CRT CHASSIS		
3	035-012	1	TV MONITOR 12", ASS'Y	BALL BROS.-TV-A12(2-030-03110)	
4	802-010	3	8-32 HEX NUT	ESNA-22 NM-82	
5	810-005	6	6-32 x 5/16 SCREWS	SEMS	

PREPARED	P. George	11-7-73
CHECKED		
APPROVED		

TITLE ASSEMBLY, CRT

DWG. NO. 502-015 | REV. A | SHEET 2 OF 2

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY PWB MAIN CHASSIS	6-002-0500	
2		1	ASSEMBLY LOW VOLTAGE CIRCUIT BOARD	6-002-0459	
3		1	ASSEMBLY HIGH VOLTAGE TRANSFORMER	6-003-0320	T2
4		1	ASSEMBLY VERTICAL CHOKE	6-003-0321	L1
5		1	ASSEMBLY 120V POWER SUPPLY MODULE	6-003-0371	
6		1	RIVETED ASSEMBLY POWER		
7			TRANSFORMER BRACKET	6-006-0226	
8		1	ASSEMBLY DEFLECTION COIL	6-004-0314	YOKE
9					
10		1	WELDED ASSEMBLY FRAME	6-006-0225	
11		1	MONITOR 12" TV-A12 MISC	1-014-0737	

PREPARED		TITLE	TOP ASSEMBLY - MONITOR
CHECKED		DWG. NO. 035-012	REV. — SHEET 1 OF 1
APPROVED			

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
		1	ASSEM PWP MAIN CHASSIS	6-002-0500	
1		1	PRINTED WIRING BOARD MAIN CHASSIS	1-029-0369	
2		1	RESISTOR WIREWOUND 1.2 ohm 2W 10%	1-011-1395	R130
3		1	RESISTOR WIREWOUND 3.3 ohm 2W 10%	1-011-1571	R125
4		1	RESISTOR COMP. 5.6 ohm 1/2 W 5%	1-011-2218	R129
5		2	RESISTOR CARBON 47 ohm 1/2 W 5%	1-011-2238	R111, R109
6		2	RESISTOR CARBON 150 ohm 1/2W 5%	1-011-2250	R114, R123
7		1	RESISTOR CARBON 220 ohm 1/2 W 5%	1-011-2254	R112
8		1	RESISTOR CARBON 390 ohm 1/2 W 5%	1-011-2260	R126
9		2	RESISTOR CARBON 470 ohm 1/2 W 5%	1-011-2262	R127, R113
10		1	RESISTOR CARBON 560 ohm 1/2W 5%	1-011-2264	R120
11		1	RESISTOR CARBON 820 ohm 1/2W 5%	1-011-2268	R110
12		2	RESISTOR CARBON 2.7K ohm 1/2W 5%	1-011-2280	R101, R128
13		1	RESISTOR CARBON 3.3K ohm 1/2W 5%	1-011-2282	R131
14		2	RESISTOR CARBON 4.7K ohm 1/2W 5%	1-011-2286	R117, R122
15		1	RESISTOR CARBON 8.2K ohm 1/2W 5%	1-011-2292	R118
16		2	RESISTOR CARBON 82K ohm 1/2W 5%	1-011-2316	R115, R103
17		3	RESISTOR CARBON 100K ohm 1/2W 5%	1-011-2318	R104, R106, R119
18		1	RESISTOR WIREWOUND 82 ohm 3W 10%	1-011-2375	R132
19		1	RESISTOR COMP. 33K ohm 1W 5%	1-011-2448	R137
20		1	RESISTOR VAR. COMP. 100 ohm 1/8W 20%	1-011-5095	R124
21		1	RESISTOR VAR. COMP. 10K ohm 1/8 W 20%	1-011-5312	R121
22		1	RESISTOR VAR. COMP. 100K ohm 1/8 W 20%	1-011-5435	R116
23		1	RESISTOR VAR. COMP. 2.5M ohm 1/8W 20%	1-011-5566	R107
24		1	ARC GAP CERAMIC .75pf 1000V	1-012-0110	C103

PREPARED			TITLE ASSEM. PWB MAIN CHASSIS, CRT	ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 6-002-0500	REV.	SHEET 1 OF 3
APPROVED				

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
25		2	ARC GAP CERAMIC .01uf 1000V	1-012-0112	C101,C102
26		1	CAP. MICA 820pf 500V 5%	1-012-0482	C118
27		1	CAP. CERAMIC .001uf 1000V 10%	1-012-0540	C104
28		1	CAP. CERAMIC .01uf 500V 20%	1-012-0740	C120
29		1	CAP. CERAMIC .02uf 500V 20%	1-012-0780	C111
30		1	CAP. MYLAR .022uf 400V 10%	1-012-0800	C109
31		1	CAP. METAL/MYLAR .1uf 200V 10%	1-012-0870	C110
32		2	CAP MYLAR .47uf 100V 10%	1-012-1005	C105, C106
33		1	CAP MYLAR 10uf 50V 10%	1-012-1130	C113
34		1	CAP ELECTROLYTIC 50uf 50V	1-012-2157	C112
35		1	CAP ELECTROLYTIC 500 uf 6V	1-012-2158	C107
36		1	CAP ELECTROLYTIC 200uf 25V	1-012-2159	C114
37		1	CAP ELECTROLYTIC 100uf 6V	1-012-2160	C108
38		1	CAP ELECTROLYTIC 50uf 25V	1-012-2165	C115
39		1	CAP ELECTROLYTIC 25uf 50V	1-012-2193	C119
40		1	TRANSISTOR 2N4124	1-015-1139	Q107
41		1	TRANSISTOR MJE3055	1-015-1156	Q104
42		1	TRANSISTOR PUT 2N6027CD1311	1-015-1157	Q102
43		1	TRANSISTOR MPS-A14	1-015-1158	Q103
44		1	TRANSISTOR MPS-V05	1-015-1159	Q105
45		1	TRANSISTOR SP2597/MP3791	1-015-1160	Q106
46		1	TRANSISTOR 2N5830	1-015-1172	Q101
47		1	HEAT SINK T077	1-015-5032	
48		1	HEAT SINK T03	1-015-5033	

PREPARED			TITLE ASSEM. PWB MAIN CHASSIS, CRT			ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 6-002-0500	REV.	SHEET 2 OF 3	
APPROVED						

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
49		1	COIL ADJ WIDTH	1-016-0303	L101
50		1	TRANSFORMER HORIZ. DRIVE	1-017-5338	T101
51		1	DIODE ZENER 1N758 10V	1-021-0180	VR101
52		1	DIODE 1N4785	1-021-0360	CR103
53		4	DIODE 1N3279	1-021-0380	CR104,105,106,107
54		3	DIODE A9201/1N3605	1-021-0410	CR101,102,108
55		1	SOCKET CRT 7 PIN	1-022-0427	
56		18	CONTACT 20-22 AWG MALE	1-034-0288	
57		1	MCH SCR 4-40 x 1/2 PHLPAN	3-011-0140	
58		4	MCH SCR 6-32 x 3/8 PHLPAN	3-011-0330	
59		1	NUT HEX 4-40 STLCAD	3-012-0140	
60		4	NUT HEX 6-32 STLCAD 1/4 FLATS	3-012-0161	
61		4	WASHER LOCK #6 INT STLCAD	3-013-0160	
62		2	RESISTOR CARBON 22K 1/4 W 5%	70-16-0223	R135,R136
63		1	RESISTOR CARBON 4.7K 1/4W 5%	70-16-0472	R133

PREPARED		TITLE ASSEM. PWB MAIN CHASSIS, CRT	ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			
APPROVED		DWG. NO. 6-002-0500 REV. SHEET 3 OF 3	

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY LOW VOLTAGE CIRCUIT BOARD	6-002-0459	
2					
3		1	PRINTED WIRING BOARD LOW VOLTAGE	1-029-0367	
4					
5		1	RESISTOR WIREWOUND .068 ohm ZW 10%	1-011-2217	R204
6		3	RESISTOR CARBON 470 ohm 1/2W 5%	1-011-2262	R206,207,209
7		2	RESISTOR CARBON 1K ohm 1/2W 5%	1-011-2270	R201,202
8		1	RESISTOR CARBON 1.5K ohm 1/2W 5%	1-011-2274	R205
9		1	RESISTOR CARBON 10K 1/2W 5%	1-011-2294	R203
10					
11		1	RESISTOR VAR COMP. 500 ohm 1/8W	1-011-5604	R208
12					
13		1	CAP. CERAMIC .01uf 500V 20%	1-012-0740	C202
14		2	CAP. ELECTROLYTIC 50 uf 50V	1-012-2157	C201,C203
15					
16					
17		2	TRANSISTOR 2N3903	1-015-1132	Q202,Q203
18		1	TRANSISTOR 2N3053	1-015-1143	Q201
19					
20		1	DIODE ZENER 1N752 5 6V	1-021-0412	VR201
21					
22		7	CONTACT -20-22 AWP MALE	1-034-0288	
23					
24		1	INSULATOR-TRANSPAD TO-5	3-019-0134	

PREPARED		
CHECKED		
APPROVED		

TITLE ASSEM. LOW VOLTAGE CIRCUIT BOARD, CRT

DWG. NO. 6-002-0459 | REV. | SHEET 1 OF 1

ADDS Applied Digital Data System, Inc. Hauppauge, New York

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY HIGH VOLTAGE TRANSFORMER	6-003-0320	T2
2					
3		2	CORE, FERRITE	1-017-5371	
4					
5		1	TRANSFORMER HIGH VOLTAGE	1-017-5372	
6					
7		1	COIL FORM	1-017-5387	
8					
9		1	DIODE H510	1-021-0424	
10					
11		1	LEAD ELEC. CRT 8.5 INCH	1-033-0163	
12					
13		5	CONTACT 20-22 AWG FEMALE	1-034-0289	
14		2	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	
15					
16		1	CLAMP FERRITE CORE 2.0 INCH	2-050-0168	
17					
18		1	INSULATION SLEEVING SHRINKABLE 2-3/8 x $\frac{1}{4}$	2-052-0187	
19					
20		2	NUT THREADING .094 STUD	3-012-0278	
21					
22		2	SHEET MYLAR 10MIL 1/4 SO	5-011-0124	

PREPARED			TITLE ASSEMBLY HIGH VOLTAGE TRANSFORMER, CRT	**ADDS** Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 6-003-0320 REV. SHEET 1 OF 1	
APPROVED				

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY VERTICAL CHOKE	6-003-0321	L1
2					
3		1	CHOKE VERTICAL	1-031-0131	
4					
5		2	CONTACT 20-22 AWG FEMALE	1-034-0289	
6					
7		1	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	

8-24

PREPARED			TITLE ASSEMBLY VERTICAL CHOKE, CRT	ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 6-003-0321 REV. SHEET OF	
APPROVED				

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY 120V POWER SUPPLY MODULE	6-003-0371	
2					
3		1	CAP ELECTROLYTIC 3300 uf 60V	1-012-2156	C1
4					
5		1	TRANSISTOR 2N3055	1-015-1134	Q1
6		1	INSULATOR MICA TO-3	2-015-5010	
7					
8		1	TRANSFORMER 120/220 VAC 50/60Hz	1-017-5390	T1
9					
10		1	DIODE BRIDGE ZA VS148	1-021-0413	CR1
11					
12		1	FUSEHOLDER 1/4 x 1-1/4	1-028-0210	
13		1	FUSE .6A-250V SLO-BLO	1-028-0244	
14					
15		7	CONTACT 20-22 AWG FEMALE	1-034-0289	
16		3	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	
17		4	CONTACT 20-22 AWG MALE	1-034-0295	
18		1	CONNECTOR SHELL 4 CONTACT FEMALE	1-034-0297	
19					
20		2	INSULATOR BUSHING NYLON .5 MTG HOLE	2-046-0230	
21					
22		1	MCH SCR 6-32 x 1/2 STLCAD PHLPAN	3-011-0352	
23		2	TPG SCR CHS CAD 6 x 1/2 PHL PAN	3-011-0408	
24		2	MCH SCR 8-32 x 1/2 STLCAD PHLPAN	3-011-0555	
25		1	NUT HEX 6-32 STLCAD 5/16 FLATS	3-012-0160	
26		1	WASHER LOCK #6 INT STLCAD	3-013-0160	
27		2	WASHER LOCK #6 INT STLCAD	3-013-0182	

PREPARED		
CHECKED		
APPROVED		

TITLE ASSEMBLY 120V POWER SUPPLY MODULE, CRT

DWG. NO. 6-003-0371 | REV. | SHEET 1 OF 1

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	RIVETED ASSEM. PWR. TRANSFORMER BKT.	6-006-0226	
2					
3		1	SOCKET TRANSISTOR POWER TO-3	1-022-0230	
4		1	SOCKET CAP. ELYTIC 1-3/8 PHEN.	1-022-0404	
5					
6		1	TERMINAL STRIP 7 LUG-2 GND #6 MTG	1-029-0145	
7					
8		1	BRACKET, POWER SUPPLY	2-017-0658	
9					
10		6	RIVET .120 x 7/32 STLCAD	3-014-0135	
11					
12		5	NUT CLINCH 8-32 STLCAD	3-019-0115	

PREPARED			TITLE RIVETED ASSEM. PWR. TRANSFORMER BKT.CRT		
CHECKED			DWG. NO. 6-006-0226	REV.	SHEET 1 OF 1
APPROVED					

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY DEFLECTION COIL	6-004-0314	
2					
3		1	COIL DEFLECTION	1-023-0205	
4					
5		4	CONTACT 20-22 AWG FEMALE	1-034-0289	
6					
7		2	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	

PREPARED			TITLE ASSEMBLY DEFLECTION COIL, CRT	ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 6-004-0314 REV. SHEET 1 OF 1	
APPROVED				

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	RIVET ASSEMBLY FRAME	6-006-0225	
2					
3		1	FRAME TV-A12	2-017-0638	
4					
5		2	GUSSET CORNER 1 FRAME	2-017-0585	
6		2	GUSSET CORNER 2 FRAME	2-017-0586	
7					
8		1	PLATE FRAME	2-017-0636	
9					
10		1	WIRE FORMED SUPPORT	2-022-0101	
11		1	WIRE FORMED U SHAPE	2-022-0131	
12		2	WIRE FORMED U SHAPE	2-022-0132	
13		1	WIRE STRAIGHT 9.5 Lg.	2-022-0133	
14		2	WIRE STRAIGHT 1.580	2-022-0134	
15					
16					
17		4	NUT CLINCH 8-32 STLCAD	3-019-0115	
18		3	NUT CLINCH 6-32 STLCAD	3-019-0119	

PREPARED		
CHECKED		
APPROVED		

TITLE: RIVETED ASSEM. FRAME, CRT

DWG. NO. 6-006-0225 | REV. | SHEET 1 OF 1

ADDS — Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	CRT 12 INCH 90° P4 BONDED LONG NECK	1-014-0737	
2					
3		1	SLEEVE LINEARITY	1-023-5035	
4					
5		7	CONTACT 20-22 AWG FEMALE	1-034-0289	
6		3	CONNECTOR SHELL 1 CONTACT MALE	1-034-0300	
7		2	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	
8					
9		1	CLAMP LOOP .187 x .287	2-050-0170	
10					
11		1	SPRING DAG 1/4 OD 6-1/2 LG	3-015-0105	
12					
13		1	TERMINAL LUG SOLDER # 6	3-016-0140	
14					
15		8	STANDOFF PCB HEIGHT 3/8	3-019-0143	

PREPARED			TITLE MONITOR 12" TV-A12 MISC.		
CHECKED			DWG. NO. 1-014-0737	REV.	SHEET 1 OF 1
APPROVED					

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

9. KEYBOARD SUBASSEMBLY

The keyboard is a subassembly which may be simply removed from a 580 for repair or replacement.

9.1 Keyboard Mechanical Package

Figure 9.1 is a mechanical drawing of the keyboard subassembly, giving overall dimensions.

Note that the keyboard can be removed from a 580 by disconnecting an edge connector at the front of the keyboard and removing four Phillips head screws at the corners of the keyboard which hold it on mounting brackets in the terminal. Field maintenance usually consists of removing a defective keyboard and replacing it with a spare unit.

Individual key modules can be replaced by desoldering two connections on the bottom P.C. board, pulling the bad module up through the hole in the mounting frame and then inserting a new module and resoldering the two P.C. board connections. Integrated circuits are located on the keyboard P.C. board so that they can generally be replaced without further board disassembly.

9.2 Keyboard Electronics

A block diagram of the keyboard electronics is presented in Figure 9.2 and a detailed schematic drawing in Figure 9.3.

The keyboard encoder is based on a scanning technique employing an 8 bit counter, a multiplexer and a 4-to-16 line decoder. Encoded keys form a crosspoint matrix with each key connected to the decoder output and the multiplexer input. The decoder is addressed by the 4 least significant bits of the counter.

When an encoded key is depressed a matrix connection between the decoder and multiplexer is accomplished. When the counter reaches the appropriate key code, the multiplexer output goes high and a retriggerable one-shot is fired on the trailing edge of the counter clock stopping the counter. The one-shot is continually refreshed until the key is released.

The bit-shift logic translates the counter address into an upper case data word, into a control data word, or into an upper case control data word if the shift and/or control key is depressed.

All keys in the array are encoded except for two function keys, BREAK and REPEAT. The function keys are de-bounced from a free running oscillator triggering a quad-D flip flop. When a function key is depressed the corresponding interface pin goes from Ground to +5 Volts and remains at +5 Volts until the key is released.

The keyboard could be "disabled" by grounding the connector pin labeled "lock-out" which disables the "strobe" output signal and all function keys. However, the Lockout function in the Consul 580 is not accomplished in this manner: this pin is left unconnected in the 580 wiring harness and the keyboard keys are always active. The 580 Lockout function is accomplished in the Front End electronics so that a keyboard action (BREAK) can be used to reset the Lockout condition.

9.3 Keyboard Interface Signals

The edge connector on the keyboard is a 30-pin connector of which only 12 pins are used. They are, from left to right;

Top Side

Pin	Signal
1	GND
2	+5 V
5*	Lockout
6	Break
9	Repeat

(3,4,7,8,10,11,12,13 14,15 are unused in top row)

*Not connected in Consul 580 wiring harness.

Bottom Side

Pin	Signal
J	Output Strobe
K	Bit 7
L	Bit 6
M	Bit 5
N	Bit 4
P	Bit 3
R	Bit 2
S	Bit 1

(A,B,C,D,E,F,H not used in bottom row)

Signals are normally at Ground and go to +5 Volts when the corresponding key is depressed.

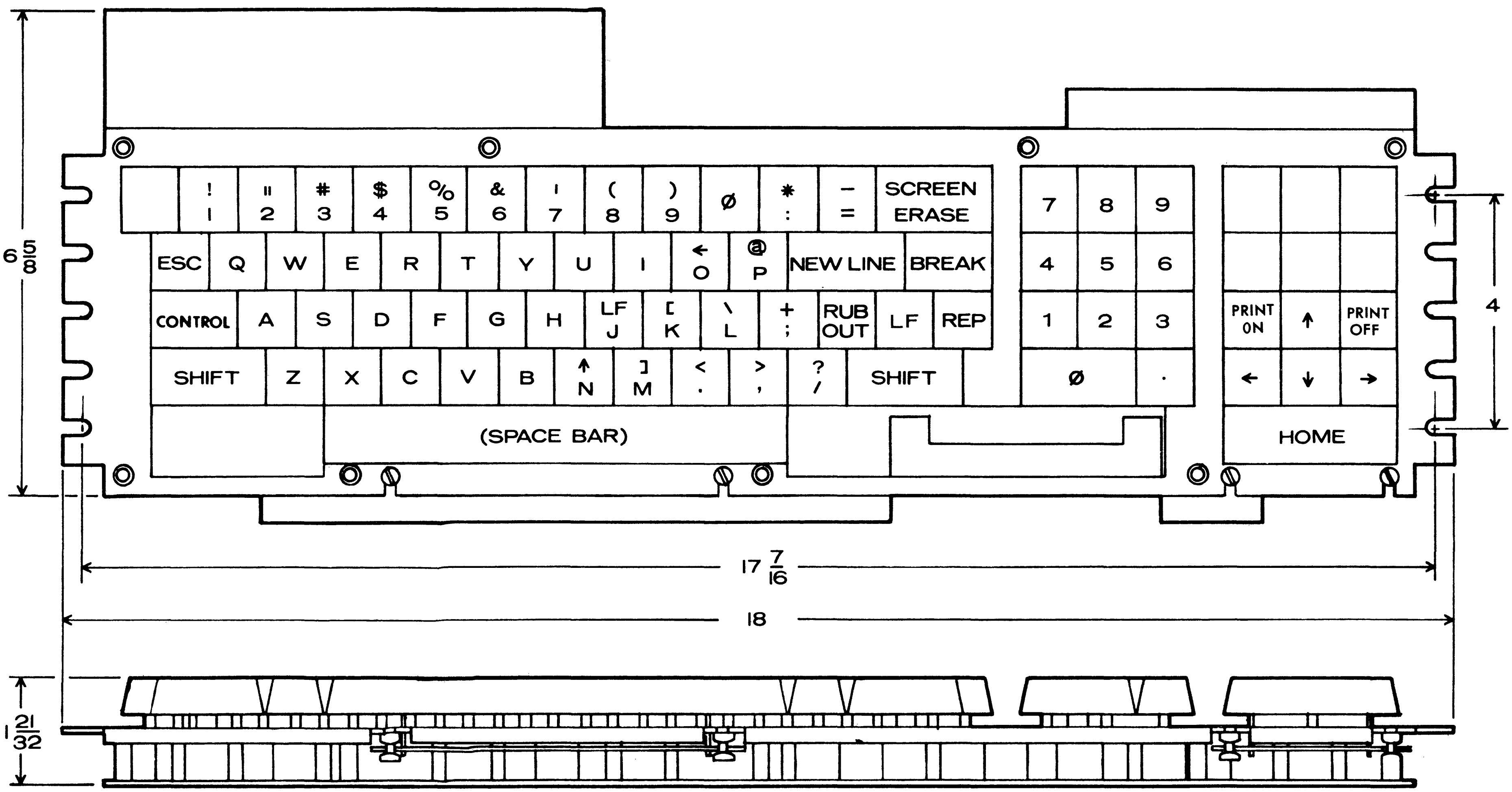
If an encoded key is depressed the Keyboard Strobe signal (KBSTB) goes to+5 Volts after the data lines become stable. The logical true data lines and the Strobe line remain at +5 Volts until the key is released.

By "logical true" we mean that the following convention applies to the seven data lines:

Logical State	Voltage
0	Ground
1	+5 Volts

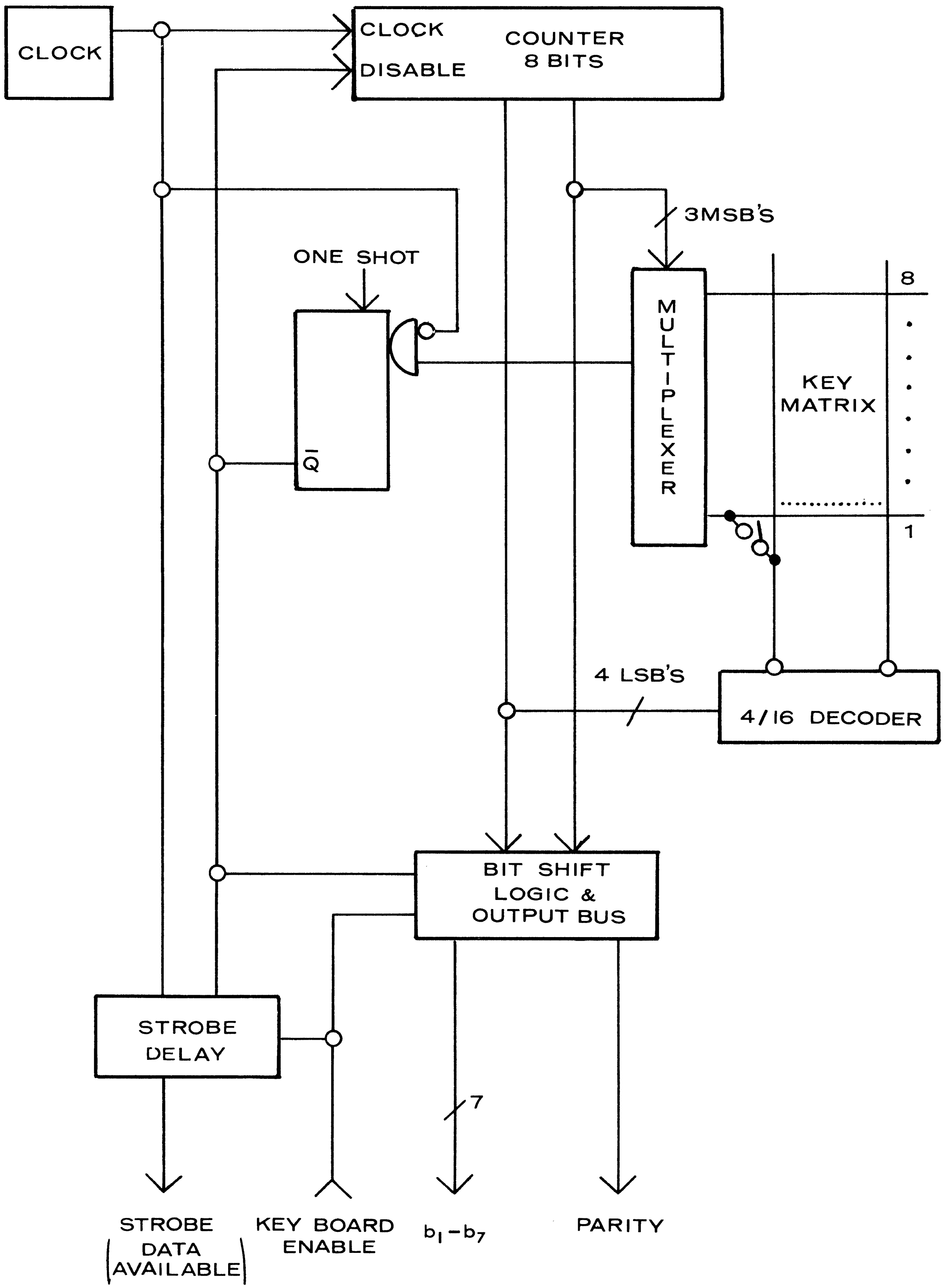
KEYBOARD DRAWING

Fig. 9·1



KEYBOARD BLOCK DIAGRAM

Fig. 9·2



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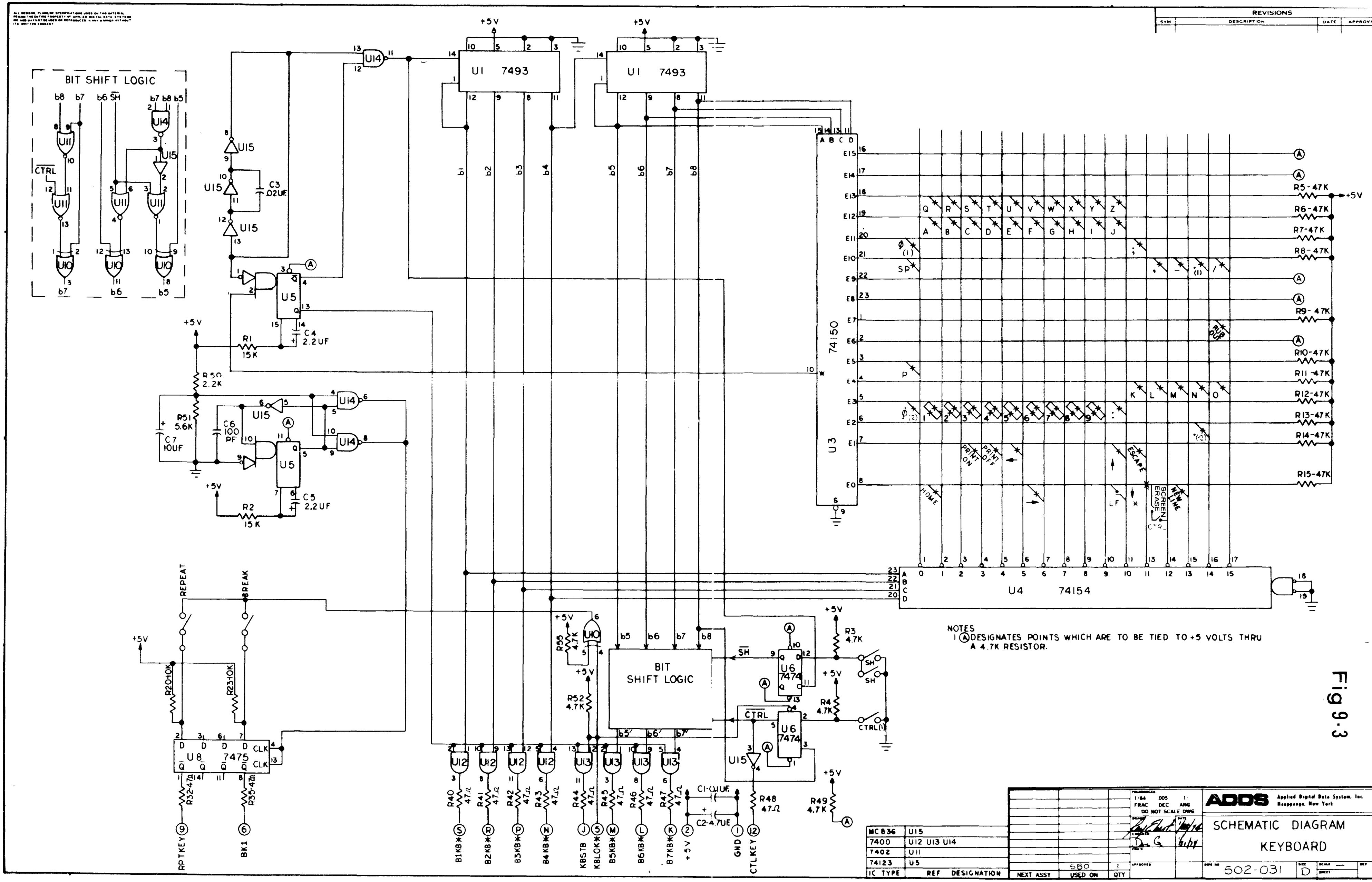


BIT SHIFT LOGIC
U1 7493
U1 7493
74150
U3
U4 74154
U5
U6 7474
U8 7475
BIT SHIFT LOGIC
REPEAT
BREAK
NOTES
1 (A) DESIGNATES POINTS WHICH ARE TO BE TIED TO +5 VOLTS THRU A 4.7K RESISTOR.
RPTKEY
BK1
B1KB*
B2KB*
B3KB*
B4KB*
KBSTB
KBLOK*
B5KB*
B6KB*
B7KB*
GND
CTLKEY
MC836 U15
7400 U12 U13 U14
7402 U11
74123 U5
IC TYPE REF DESIGNATION
NEXT ASSY
USED ON
QTY
580
1
DO NOT SCALE DWG
ADDS Applied Digital Data Systems, Inc. Hauppauge, New York
SCHEMATIC DIAGRAM
KEYBOARD
502-031
D

Fig 9.3

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	502-008A	1	ASS'Y KEYBOARD 880/800A		
2	502-703A	1	KEYBOARD MTG. BRKT. R.H.		
3	502-704D	1	KEYBOARD MTG. BRKT. L.H.		
4	502-736B	2	KEYBOARD HOLD DOWN BRKT		
5	355-007	1	KEYBOARD ASS'Y. 880/800A	CHERRY 120-0046	
6	810-005	8	6-32 x 5/16 SCREW	SEMS	
7	790-008-S-1	8	6-32 FLAT WASHER, CRS, CAD PLATE		
8	360-089	AR	CATERPILLAR TRACK		

PREPARED	P.George	11-7-73	TITLE: ASSEMBLY KEYBOARD 880/800A		
CHECKED			DWG. NO. 502-008	REV. A	SHEET 2 OF 2
APPROVED					

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	355-007	1	ASSEMBLY, KEYBOARD - 880		
2					
3		1	P.C. BOARD	CHERRY ELECT 001-0608	
4					
5		1	PLATE, COVER	CHERRY ELECT 022-0304	
6					
7	356-001	74	MODULE, MOMENTARY ACTION (BASIC KEY)	CHERRY ELECT M61-0100	
8	356-002	2	MODULE, ALTERNATE ACTION KEY (INSERT & PRINT KEY)	CHERRY ELECT M61-0800	
9	356-003	2	MODULE, MOMENTARY ACTION KEY (HOME & SPACE BAR)	CHERRY ELECT M51-0106	
10	356-004	2	ASSEMBLY, LIGHT (INSERT-PRINT-LINE KEYS)	CHERRY ELECT M10-1007	
11		4	PIN, POWER (BETWEEN LT ASSY & PC BOARD)		
12					
13	360-114	1	KEYTOP, ENGRAVED "OFF-LINE" (880A ONLY)		
14	360-113	1	KEYTOP, ENGRAVED "PRINT LINE" (880 ONLY)		
15	360-111	1	KEYTOP SET - 880 (ONLY)		
16	360-112	1	KEYTOP SET - 880A (ONLY)		
17					
18		8	SPACER	CHERRY ELECT. 013-0079	
19	360-126	2	PLUNGER, SPACE BAR	CHERRY ELECT. 004-0549	
20	360-127	2	PLUNGER, HOME KEY	CHERRY ELECT. 004-0603	
21	360-128	3	PIVOT	CHERRY ELECT. 012-0325	
22	360-129	1	PIVOT	CHERRY ELECT. 012-0565	
23	360-130	1	BRACKET, PIVOT (HOME KEY)	CHERRY ELECT. 004-0550	
24	360-131	1	BRACKET, PIVOT (SPACE BAR)	CHERRY ELECT. 004-0577	
25					
26		5	4/40 x 1/8 LG BINDING HEAD SCREW	CHERRY ELECT. 012-0324	
27					

PREPARED	TITLE KEYBOARD - 880 & 880A	ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED		
APPROVED	DWG. NO. 355-007 REV. D SHEET 1 OF 2	

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
28	200-006	3	INTEGRATED CIRCUIT - 7400	NATIONAL/T.I.	U12,U13,U14
29	200-002	1	INTEGRATED CIRCUIT - 7402	NATIONAL/T.I.	U11
30	200-008	1	INTEGRATED CIRCUIT - 7474	NATIONAL/T.I.	U6
31	200-016	3	INTEGRATED CIRCUIT - 7475	NATIONAL/T.I.	U7,U8,U9
32	200-074	1	INTEGRATED CIRCUIT - 7486	NATIONAL/T.I.	U10
33	200-027	2	INTEGRATED CIRCUIT - 7493	NATIONAL/T.I.	U1,U2
34	200-080	1	INTEGRATED CIRCUIT - 74123	NATIONAL/T.I.	U5
35	200-081	1	INTEGRATED CIRCUIT - 74150	NATIONAL/T.I.	U3
36	200-082	1	INTEGRATED CIRCUIT - 74154	NATIONAL/T.I.	U4
37	200-083	1	INTEGRATED CIRCUIT - 15836	NATIONAL/T.I.	U15
38					
39		21	RESISTOR, COMP 47 ohm 1/4W 5%		R28 thru R48
40		3	RESISTOR, COMP 2.2K		R50,R53,R54
41		16	RESISTOR, COMP 4.7K		R3 thru R15,R49,52,55
42		1	RESISTOR, COMP 5.6K		R51
43		12	RESISTOR, COMP 10K		R16 thru R27
44		2	RESISTOR, COMP 15K		R1,R2
45					
46		1	CAPACITOR, DISC. .02uf, 20%, 16V	RMC	
47		1	CAPACITOR, DISC. .1 uf 20%, 25V	RMC	
48		1	CAPACITOR, TANT 4.7 uf, 20%, 6V	SPRAGUE 150D	
49		2	CAPACITOR, TANT 2.2 uf, 20%, 15V	SPRAGUE 150D	
50		1	CAPACITOR, TANT 10 uf, 20%, 20V	SPRAGUE 150D	
51					
52		2	TRANSISTOR 2N2907 PNP	TO-18 CASE	
53					
54					

PREPARED		TITLE KEYBOARD 880 & 880A		ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED		DWG. NO. 355-007	REV. D	SHEET 2 OF 2
APPROVED				

BILL OF MATERIAL

10. SCHEMATIC AND ASSEMBLY DRAWINGS

This section includes the schematic and assembly drawings listed below.

For Units delivered after January 15, 1974

FE/GT	135-079B	Schematic
	129-079A	Assembly
VG/GT	135-080A	Schematic
	129-080	Assembly
MC/GT	135-081A	Schematic
	129-081A	Assembly

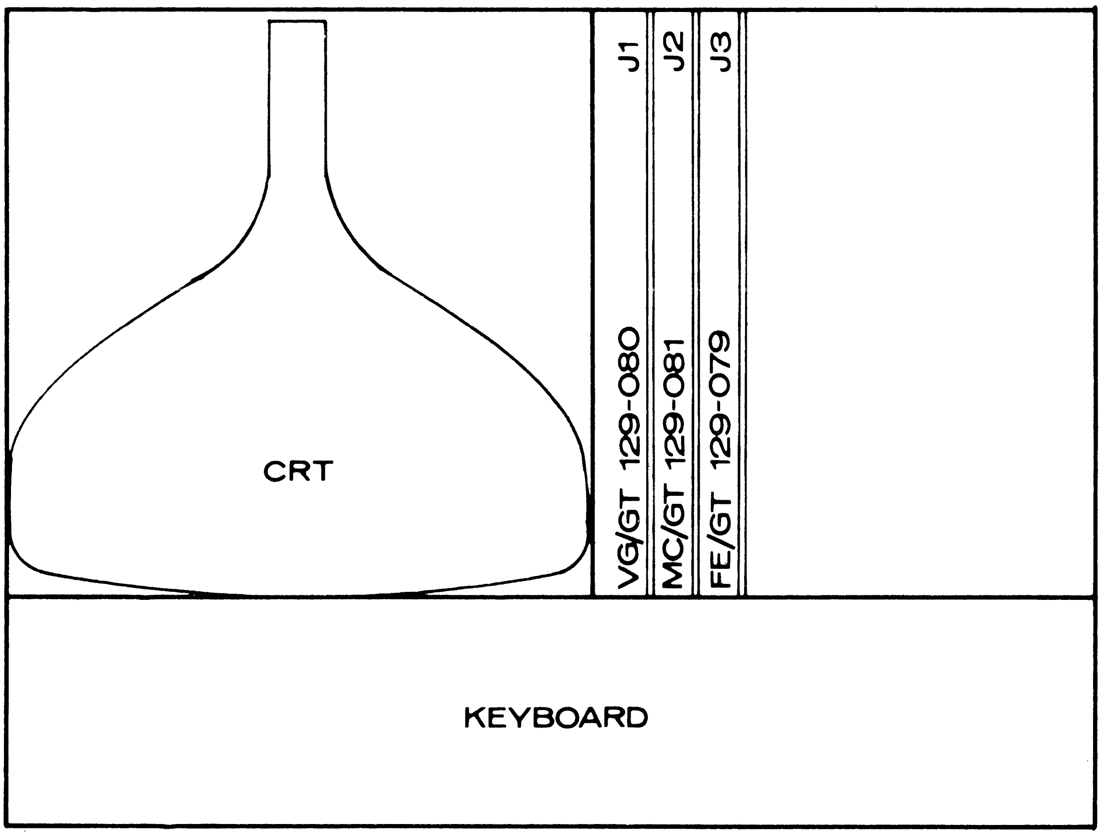
For units delivered before January 15, 1974

FE/GT	135-079	Schematic
	129-079	Assembly
VG/GT	135-080	Schematic
	129-080	Assembly
MC/GT	135-081	Schematic
	129-081	Assembly

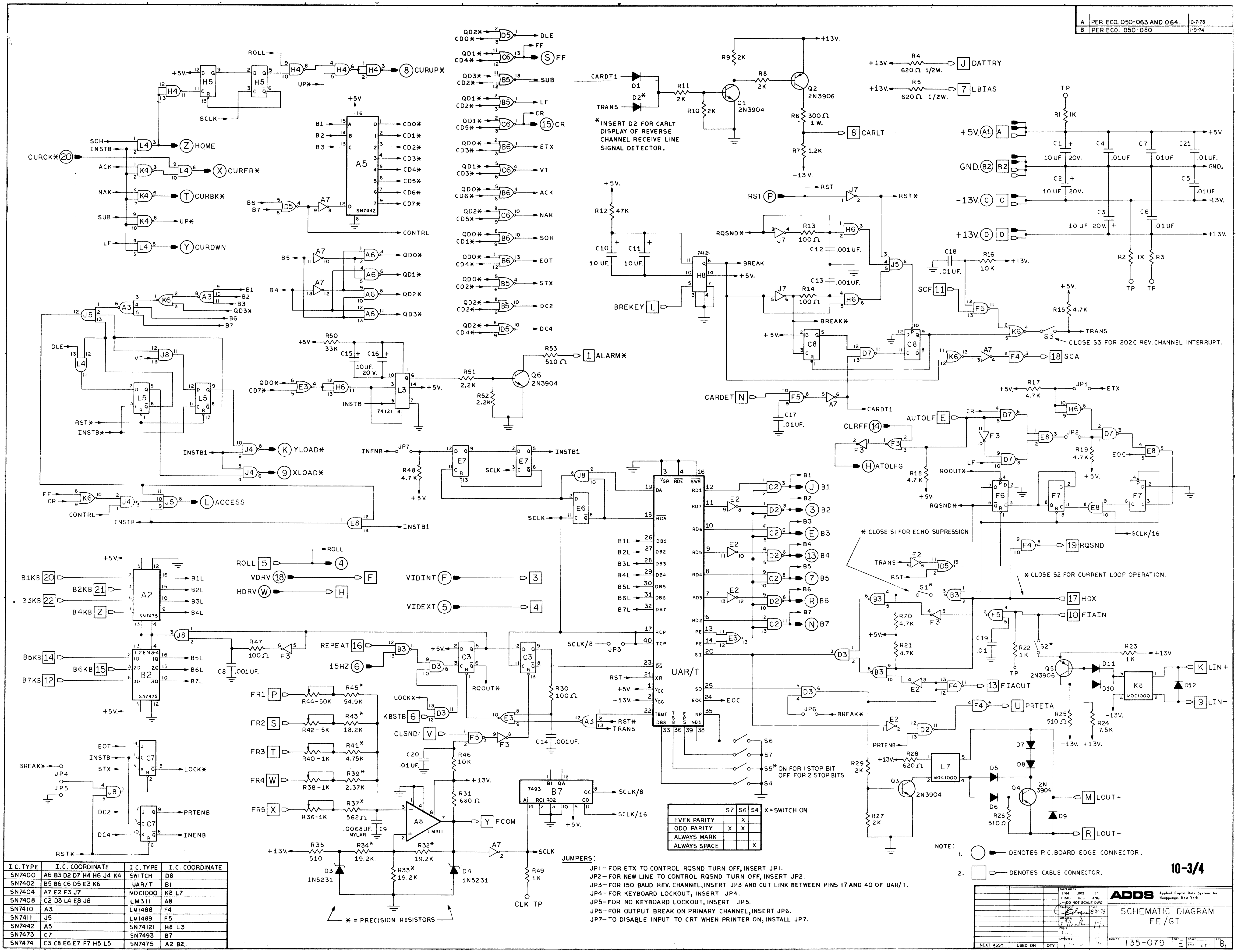
A card locator chart for the 580 is presented on page 10-2 showing P.C. board placement in the card cage.

CONSUL 580, P. C. CARD LOCATIONS

Fig. 10·1



—TOP VIEW—



	S7	S6	S4
EVEN PARITY		X	
ODD PARITY	X	X	
ALWAYS MARK			
ALWAYS SPACE			X

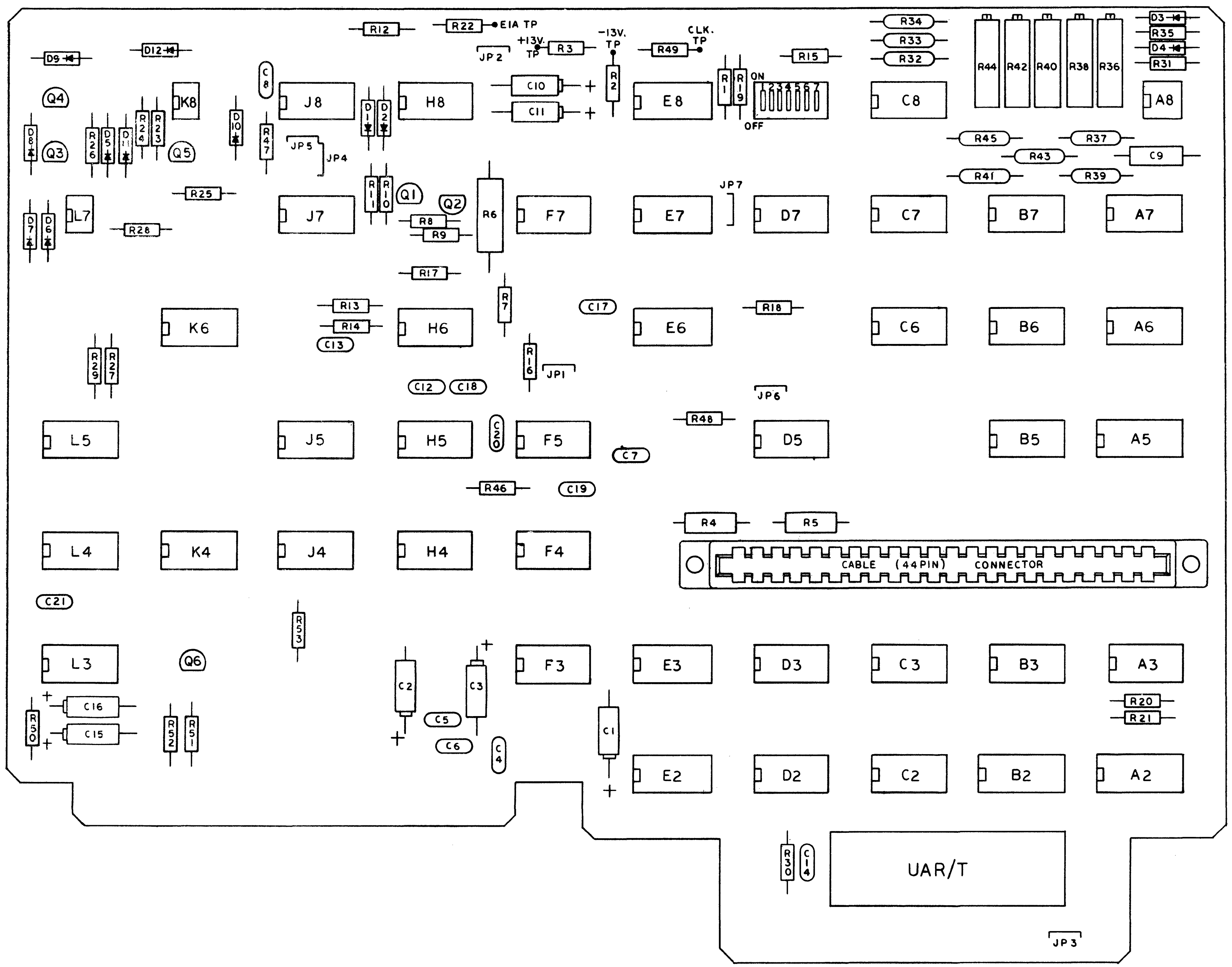
X = SWITCH ON

JUMPERS:

JP1 – FOR ETX TO CONTROL RQSND TURN OFF, INSERT JP1.
JP2 – FOR NEW LINE TO CONTROL RQSND TURN OFF, INSERT JP2.
JP3 – FOR 150 BAUD REV. CHANNEL, INSERT JP3 AND CUT LINK BETWEEN PINS 17 AND 40 OF UAR/T.
JP4 – FOR KEYBOARD LOCKOUT, INSERT JP4.
JP5 – FOR NO KEYBOARD LOCKOUT, INSERT JP5.
JP6 – FOR OUTPUT BREAK ON PRIMARY CHANNEL, INSERT JP6.
JP7 – TO DISABLE INPUT TO CRT WHEN PRINTER ON, INSTALL JP7.

I.C. TYPE	I.C. COORDINATE	I.C. TYPE	I.C. COORDINATE
SN7400	A6 B3 D2 D7 H4 H6 J4 K4	SWITCH	D8
SN7402	B5 B6 C6 D5 E3 K6	UAR/T	B1
SN7404	A7 E2 F3 J7	MOC1000	K8 L7
SN7408	C2 D3 L4 E8 J8	LM311	A8
SN7410	A3	LM1488	F4
SN7411	J5	LM1489	F5
SN7442	A5	SN74121	H8 L3
SN7473	C7	SN7493	B7
SN7474	C3 C8 E6 E7 F7 H5 L5	SN7475	A2 B2

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	PER ECO NO. 050 063 AND 064	10-15-73	



NOTES:

1. JUMPERS:

   JP1 - FOR ETX TO CONTROL RQSND TURN OFF, INSERT JP1.

   JP2 - FOR NEW LINE TO CONTROL RQSND TURN OFF, INSERT JP2.

   JP3 - FOR 150 BAUD REV. CHANNEL, INSERT JP3 AND CUT LINK BETWEEN PINS 17 AND 40 OF UAR/T.

   JP4 - FOR KEYBOARD LOCKOUT, INSERT JP4.

   JP5 - FOR NO KEYBOARD LOCKOUT, INSERT JP5.

   JP6 - FOR OUTPUT BREAK ON PRIMARY CHANNEL, INSERT JP6.

   JP7 - TO DISABLE INPUT TO CRT WHEN PRINTER ON, INSTALL JP7.

2. SWITCH:

   S1 - ON FOR ECHO SUPRESSION.

   S2 - ON FOR CURRENT LOOP OPERATION.

   S3 - ON FOR 202-C REVERSE CHANNEL INTERRUPT.

   S4 - ON FOR ODD PARITY.

   S5 - ON FOR 1 STOP BIT, OFF FOR 2 STOP BITS.

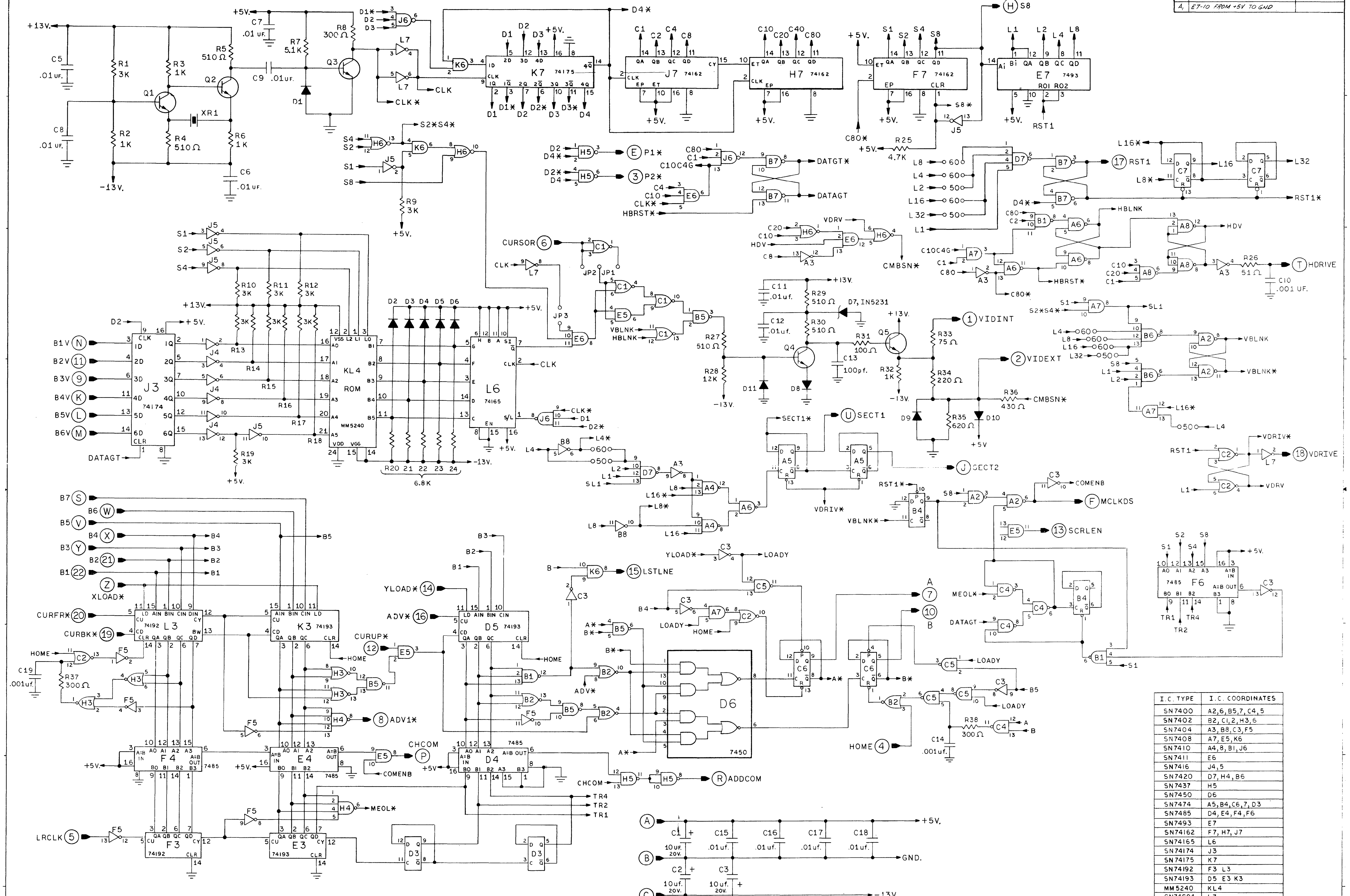
   S6 - ON FOR PARITY.

   S7 - ON FOR ALWAYS SPACE.

10-5/6

NEXT ASSY	USED ON	QTY	TOLERANCES: 1/64 FRAC .005 DEC 1° ANG DO NOT SCALE DWG		ADDS Applied Digital Data System, Inc. Hauppauge, New York
			DRAWN Bologna	DATE 10/15/73	ASSEMBLY FE/GT
			CHECKED D. Gardner	10/17/73	
			ENGR	10/17/73	
			APPROVED	10/17/73	DWG NO 129-079 SIZE D SCALE — SHEET 1 of 4 REV A

A	PER ECO. 050-081	1-9-74
A1	E7-10 FROM +5V TO GND	



I.C. TYPE	I.C. COORDINATES
SN7400	A2,6,B5,7,C4,5
SN7402	B2,C1,2,H3,6
SN7404	A3,B8,C3,F5
SN7408	A7,E5,K6
SN7410	A4,8,B1,J6
SN7411	E6
SN7416	J4,5
SN7420	D7,H4,B6
SN7437	H5
SN7450	D6
SN7474	A5,B4,C6,7,D3
SN7485	D4,E4,F4,F6
SN7493	E7
SN74162	F7,H7,J7
SN74165	L6
SN74174	J3
SN74175	K7
SN74192	F3 L3
SN74193	D5 E3 K3
MM5240	KL4
SN74S04	L7

NOTES:

1. ALL RESISTORS ARE 1/4 W, 5%, UNLESS OTHERWISE NOTED.
2. ALL DIODES ARE IN914 UNLESS OTHERWISE NOTED.
3. ALL TRANSISTORS ARE 2N3646 UNLESS OTHERWISE NOTED.
4. FOR 50 Hz OPERATION, INSTALL ONLY 50 Hz JUMPERS AND 12.6 MHz CRYSTAL.
5. FOR 60 Hz OPERATION, INSTALL ONLY 60 Hz JUMPERS AND 12.528 MHz CRYSTAL.
6. FOR BLACK CHARACTERS ON WHITE BACKGROUND, INSTALL JP1.
7. FOR WHITE CHARACTERS ON BLACK BACKGROUND, INSTALL JP2 AND JP3.

10-7/8

TOLERANCES 1/64 FRAC .005 DEC 1° ANG
DO NOT SCALE DWG
DRAWN Bologna DATE 8/15/73
CHECKED
ENG R
APPROVED

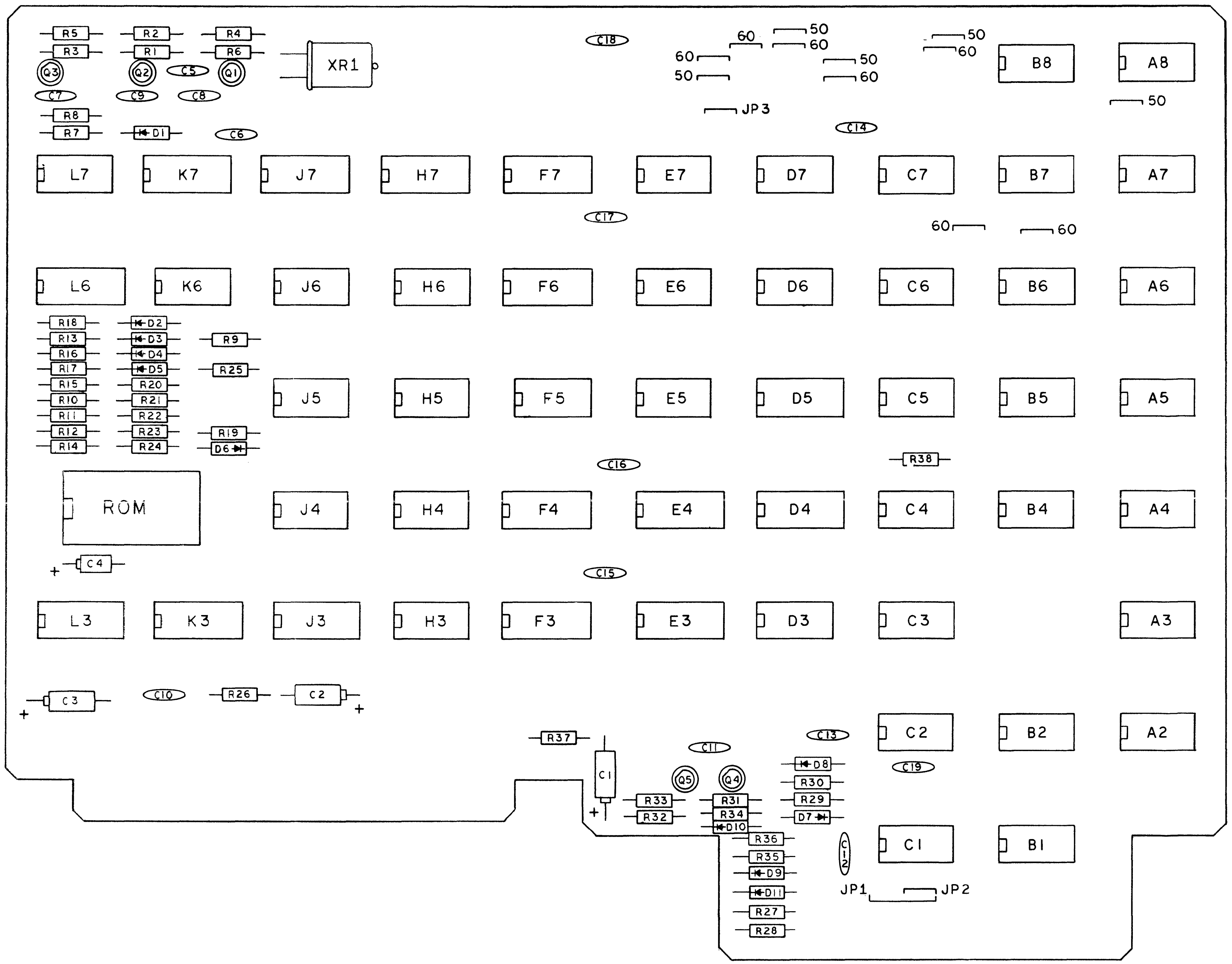
ADDS Applied Digital Data System, Inc. Hauppauge, New York

SCHEMATIC DIAGRAM
VG/GT

DWG NO 135-080 SIZE E SCALE SHEET 1 REV A1

NEXT ASSY | USED ON | QTY

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



10-9/10

NOTES:

1. FOR 50 HZ OPERATION, INSTALL ONLY 50 HZ JUMPERS AND 12.6 MHZ CRYSTAL.
2. FOR 60 HZ OPERATION, INSTALL ONLY 60 HZ JUMPERS AND 12.528 MHZ CRYSTAL.
3. FOR BLACK CHARACTERS ON WHITE BACKGROUND, INSTALL JP1.
4. FOR WHITE CHARACTERS ON BLACK BACKGROUND, INSTALL JP2 and JP3.

NEXT ASSY	USED ON	QTY

TOLERANCES: 1/64 FRAC, .005 DEC, 1° ANG
DO NOT SCALE DWG

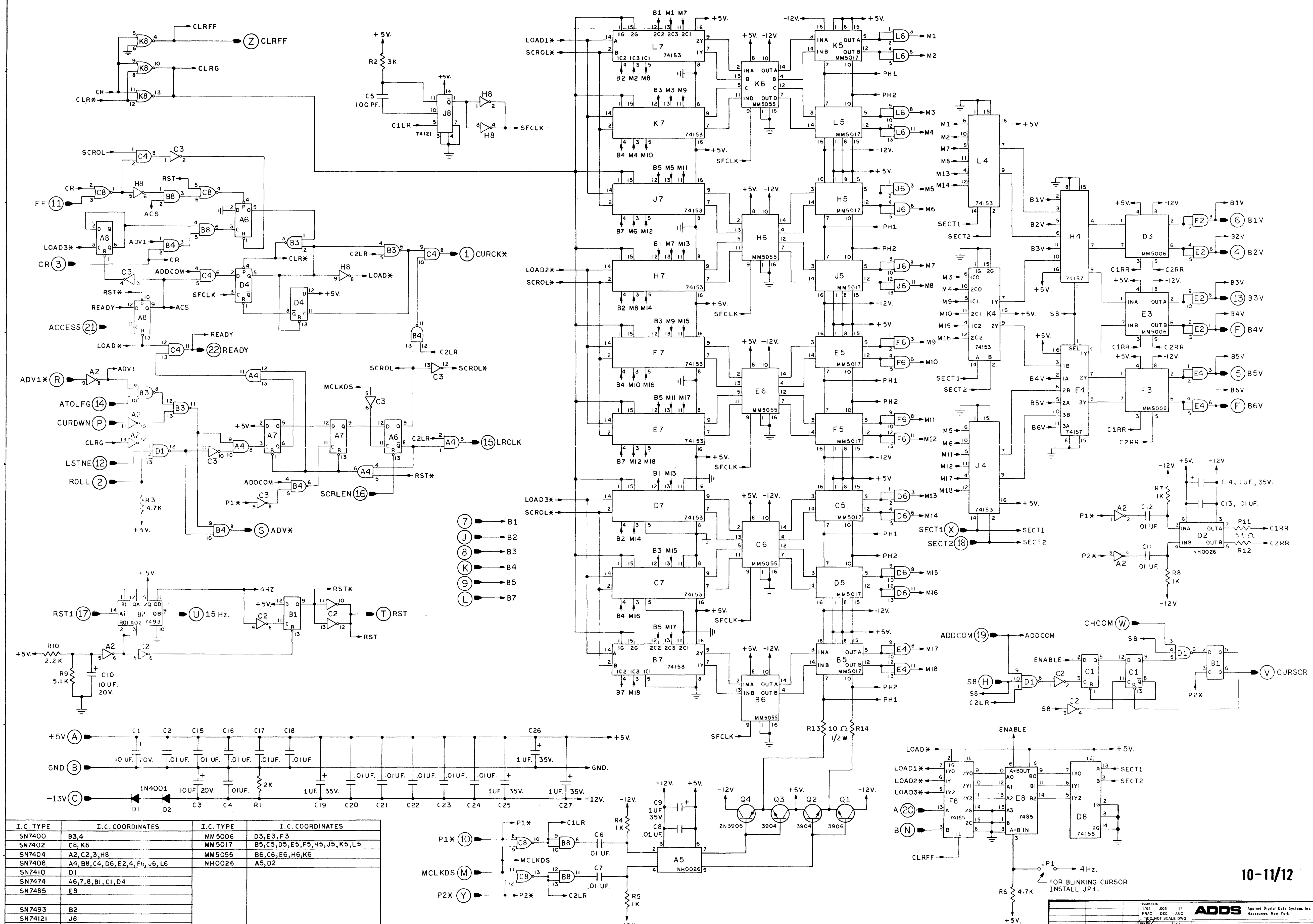
DRAWN	Bologna	10/11/73
CHECKED	Gardiner	10/17/73
ENG'R	Jacobs	10/17/73
APPROVED	Jacobs	10/17/73

ADDS Applied Digital Data System, Inc. Hauppauge, New York

ASSEMBLY VG/GT

DWG NO 129-080 SIZE D SCALE — SHEET 1 of 4 REV —

A | PER ECO. 050-062,067,069. | 10-8-73



I.C. TYPE	I.C. COORDINATES	I.C. TYPE	I.C. COORDINATES
SN7400	B3,4	MM5006	D3,E3,F3
SN7402	C8,K8	MM5017	B5,C5,D5,E5,F5,H5,J5,K5,L5
SN7404	A2,C2,3,H8	MM5055	B6,C6,E6,H6,K6
SN7408	A4,B8,C4,D6,E2,4,F6,J6,L6	NH0026	A5,D2
SN7410	D1		
SN7474	A6,7,8,B1,C1,D4		
SN7485	E8		
SN7493	B2		
SN74121	J8		
SN74153	B7,C7,D7,E7,F7,H7,J4,7,K4,7,L4,7		
SN74155	D8,F8		
SN74157	F4,H4		

10-11/12

TOLERANCES 1/64 FRAC .005 DEC 1° ANG DO NOT SCALE DWG

DRAWN [signature] DATE 8/30/73 · CHECKED [signature] · ENG R [signature] · APPROVED [signature]

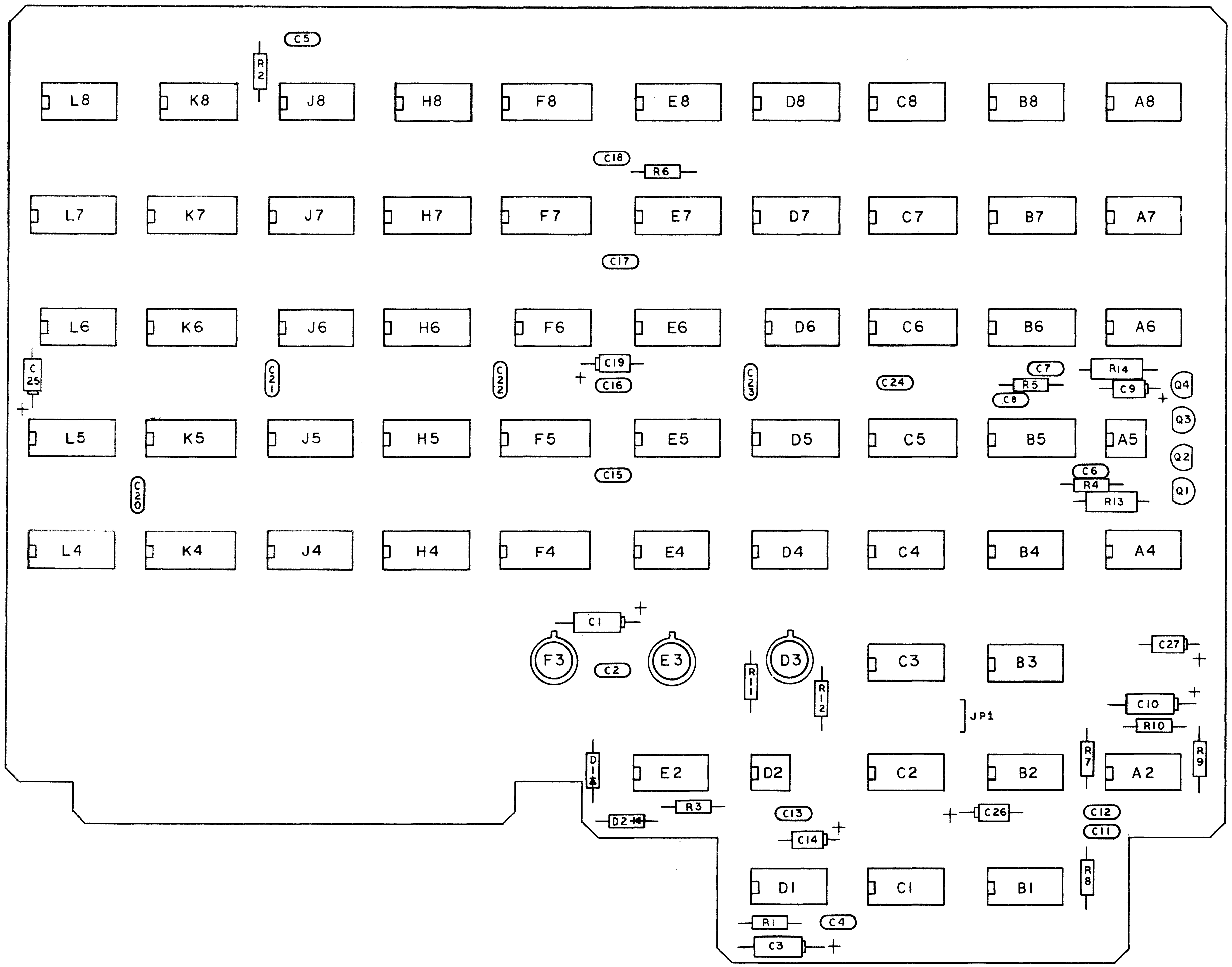
NEXT ASSY | USED ON | QTY

ADDS Applied Digital Data System, Inc. Hauppauge, New York

SCHEMATIC DIAGRAM
MC/GT

DWG NO 135-081 SIZE D SCALE — SHEET 1 of 3 REV A

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	PER ECO. NO. 050-062	10-9-73	



NOTE:

FOR BLINKING CURSOR INSTALL JP1.

10-13/14

NEXT ASSY	USED ON	QTY	

TOLERANCES: 1/64 FRAC, .005 DEC, 1° ANG

DO NOT SCALE DWG

DRAWN: Bologna — DATE: 10/13/73

CHECKED: D Gardner — 10/17/73

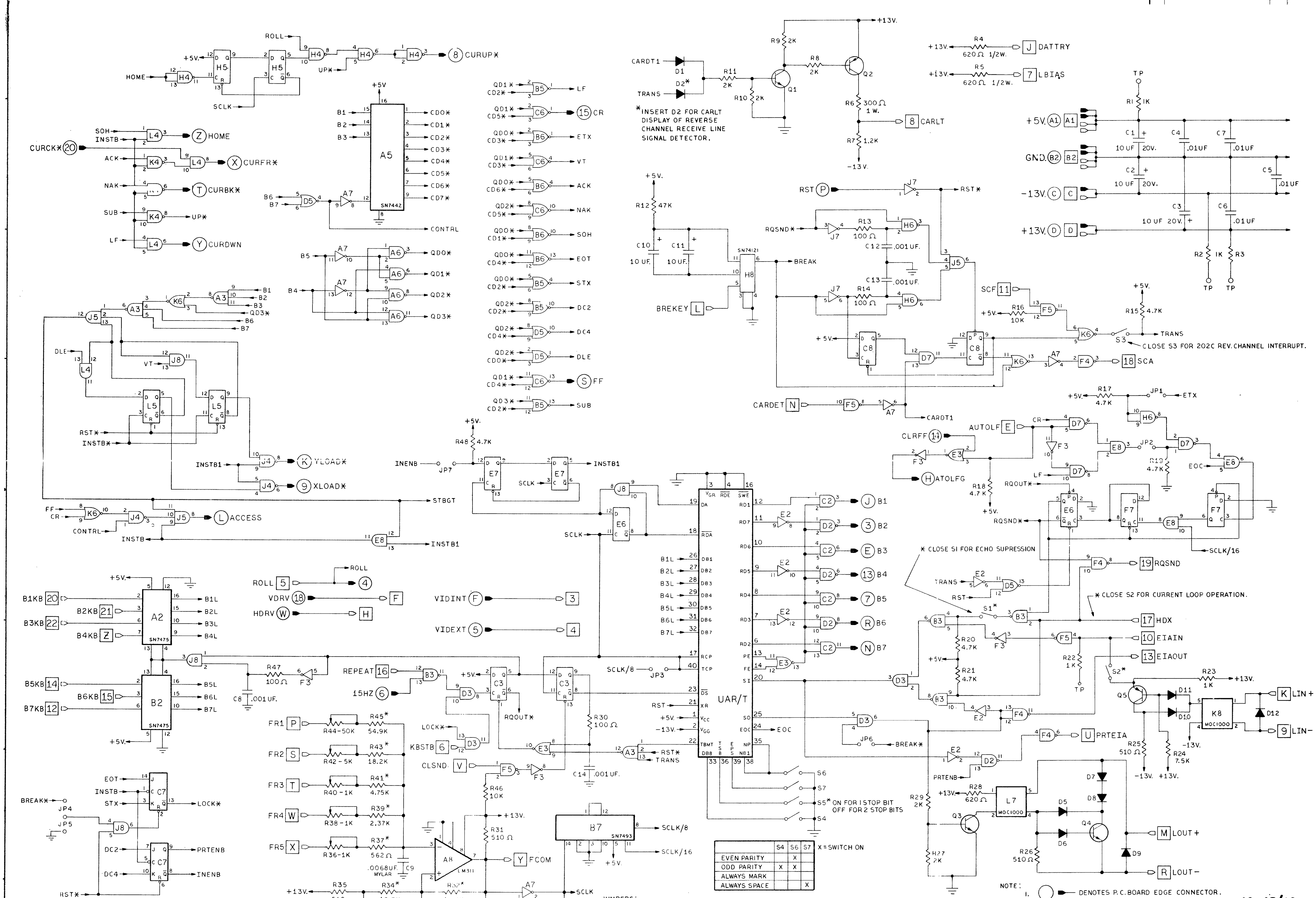
ENG'R: [signature] — 10/17/73

APPROVED: [signature] — 10/17/73

ADDS Applied Digital Data System, Inc. Hauppauge, New York

ASSEMBLY
MC/GT

DWG NO 129-081 | SIZE D | SCALE — | SHEET 1 of 3 | REV A



S	S4	S6	S7
EVEN PARITY		X	
ODD PARITY	X	X	
ALWAYS MARK			
ALWAYS SPACE			X

X = SWITCH ON

I.C. TYPE	I.C. COORDINATE	I.C. TYPE	I.C. COORDINATE
SN7400	A6 B3 D2 D7 H4 H6 J4 K4	SWITCH	D8
SN7402	B5 B6 C6 D5 E3 K6	UAR/T	B1
SN7404	A7 E2 F3 J7	MOC1000	K8 L7
SN7408	C2 D3 L4 E8 J8	LM311	A8
SN7410	A3	SN1488	F4
SN7411	J5	SN1489	F5
SN7442	A5	SN74121	H8
SN7473	C7	SN7493	B7
SN7474	C3 C8 E6 E7 F7 H5 L5	SN7475	A2 B2

JUMPERS:

JP1– FOR ETX TO CONTROL RQSND TURN OFF, INSERT JP1.
JP2– FOR NEW LINE TO CONTROL RQSND TURN OFF, INSERT JP2.
JP3– FOR 150 BAUD REV. CHANNEL, INSERT JP3 AND CUT LINK BETWEEN PINS 17 AND 40 OF UAR/T.
JP4– FOR KEYBOARD LOCKOUT, INSERT JP4.
JP5– FOR NO KEYBOARD LOCKOUT, INSERT JP5.
JP6– FOR OUTPUT BREAK ON PRIMARY CHANNEL, INSERT JP6.
JP7– TO DISABLE INPUT TO CRT WHEN PRINTER ON, INSTALL JP7.

NOTE:
1. ○ DENOTES P.C. BOARD EDGE CONNECTOR.
2. □ DENOTES CABLE CONNECTOR.

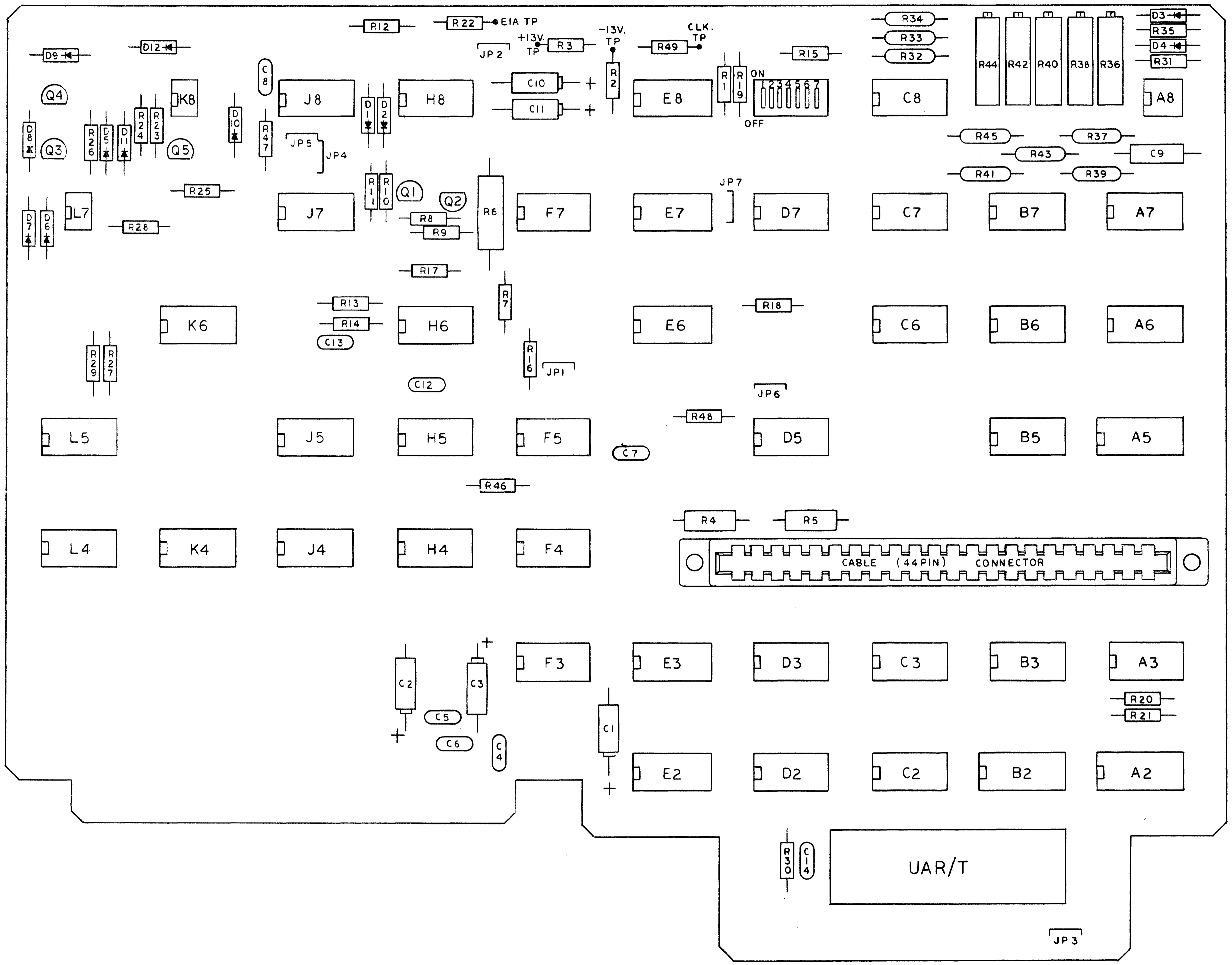
10-15/16

ADDS Applied Digital Data Systems, Inc. Hauppauge, New York

SCHEMATIC DIAGRAM FE/GT

DWG NO 135-079 SIZE E SHEET 1 of 4

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



NOTES:

1. JUMPERS:

JP1 - FOR ETX TO CONTROL RQSND TURN OFF, INSERT JP1.

JP2 - FOR NEW LINE TO CONTROL RQSND TURN OFF, INSERT JP2.

JP3 - FOR 150 BAUD REV. CHANNEL, INSERT JP3 AND CUT LINK BETWEEN PINS 17 AND 40 OF UAR/T.

JP4 - FOR KEYBOARD LOCKOUT, INSERT JP4.

JP5 - FOR NO KEYBOARD LOCKOUT, INSERT JP5.

JP6 - FOR OUTPUT BREAK ON PRIMARY CHANNEL, INSERT JP6.

JP7 - TO DISABLE INPUT TO CRT WHEN PRINTER ON, INSTALL JP7.

2. SWITCH:

S1 - ON FOR ECHO SUPRESSION.

S2 - ON FOR CURRENT LOOP OPERATION.

S3 - ON FOR 202-C REVERSE CHANNEL INTERRUPT.

S4 - ON FOR ODD PARITY.

S5 - ON FOR 1 STOP BIT, OFF FOR 2 STOP BITS.

S6 - ON FOR PARITY.

S7 - ON FOR ALWAYS SPACE.

10-17/18

NEXT ASSY	USED ON	QTY

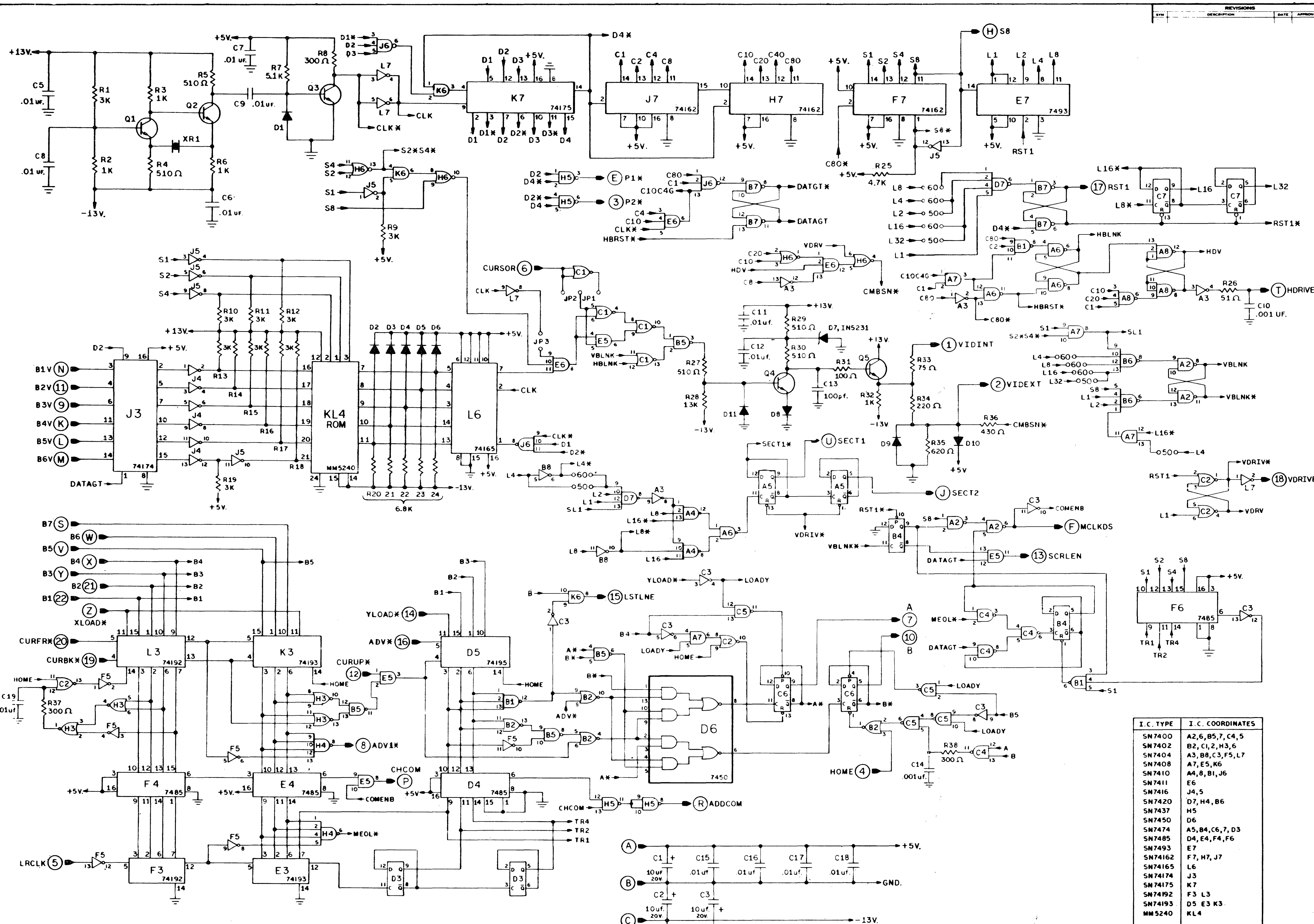
TOLERANCES: 1/64 FRAC, .005 DEC, 1° ANG
DO NOT SCALE DWG

		DATE
DRAWN	Bologna	10/15/73
CHECKED	[illegible]	10/17/73
ENG'R	[illegible]	10/17/73
APPROVED	[illegible]	10/17/73

ADDS Applied Digital Data System, Inc. Hauppauge, New York

ASSEMBLY
FE/GT

DWG NO 129-079 | SIZE D | SCALE — | SHEET 1 of 4 | REV



NOTES:

1. ALL RESISTORS ARE 1/4 W, 5%, UNLESS OTHERWISE NOTED.
2. ALL DIODES ARE IN914 UNLESS OTHERWISE NOTED.
3. ALL TRANSISTORS ARE 2N3646 UNLESS OTHERWISE NOTED.
4. FOR 50 Hz OPERATION, INSTALL ONLY 50 Hz JUMPERS AND 12.6 MHz CRYSTAL.
5. FOR 60 Hz OPERATION, INSTALL ONLY 60 Hz JUMPERS AND 12.528 MHz CRYSTAL.
6. FOR BLACK CHARACTERS ON WHITE BACKGROUND, INSTALL JP1.
7. FOR WHITE CHARACTERS ON BLACK BACKGROUND, INSTALL JP2 AND JP3.

I.C. TYPE	I.C. COORDINATES
SN7400	A2,6, B5,7, C4,5
SN7402	B2, C1,2, H3,6
SN7404	A3, B8, C3, F5, L7
SN7408	A7, E5, K6
SN7410	A4, 8, B1, J6
SN7411	E6
SN7416	J4,5
SN7420	D7, H4, B6
SN7437	H5
SN7450	D6
SN7474	A5, B4, C6,7, D3
SN7485	D4, E4, F4, F6
SN7493	E7
SN74162	F7, H7, J7
SN74165	L6
SN74174	J3
SN74175	K7
SN74192	F3 L3
SN74193	D5 E3 K3
MM5240	KL4

10-19/20

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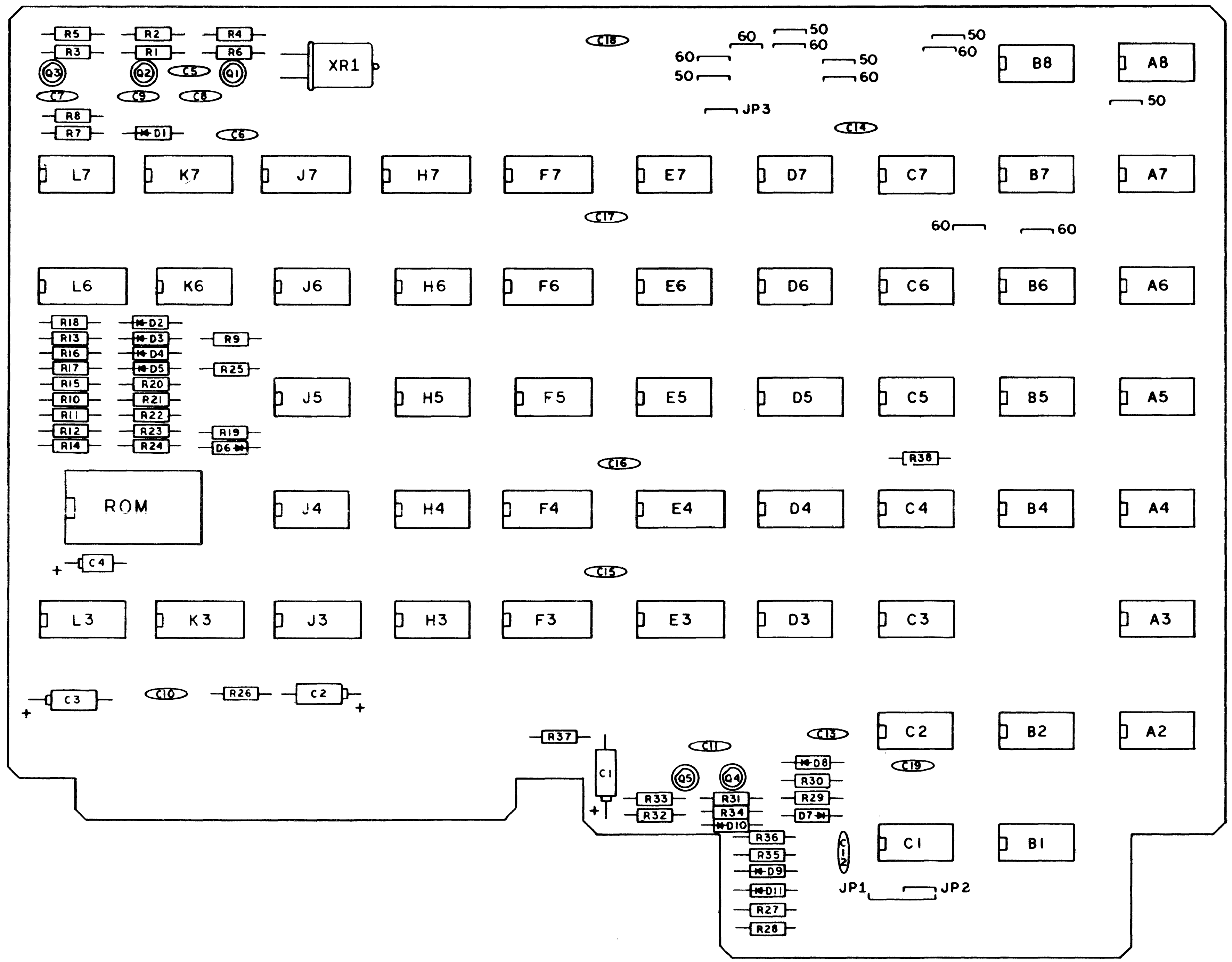
DO NOT SCALE DWG

SCHEMATIC DIAGRAM VG/GT

NEXT ASSY | USED ON | QTY

135-080 E

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



NOTES:

1. FOR 50 HZ OPERATION, INSTALL ONLY 50 HZ JUMPERS AND 12.6 MHZ CRYSTAL.
2. FOR 60 HZ OPERATION, INSTALL ONLY 60 HZ JUMPERS AND 12.528 MHZ CRYSTAL.
3. FOR BLACK CHARACTERS ON WHITE BACKGROUND, INSTALL JP1.
4. FOR WHITE CHARACTERS ON BLACK BACKGROUND, INSTALL JP2 and JP3.

10-20/21

NEXT ASSY	USED ON	QTY

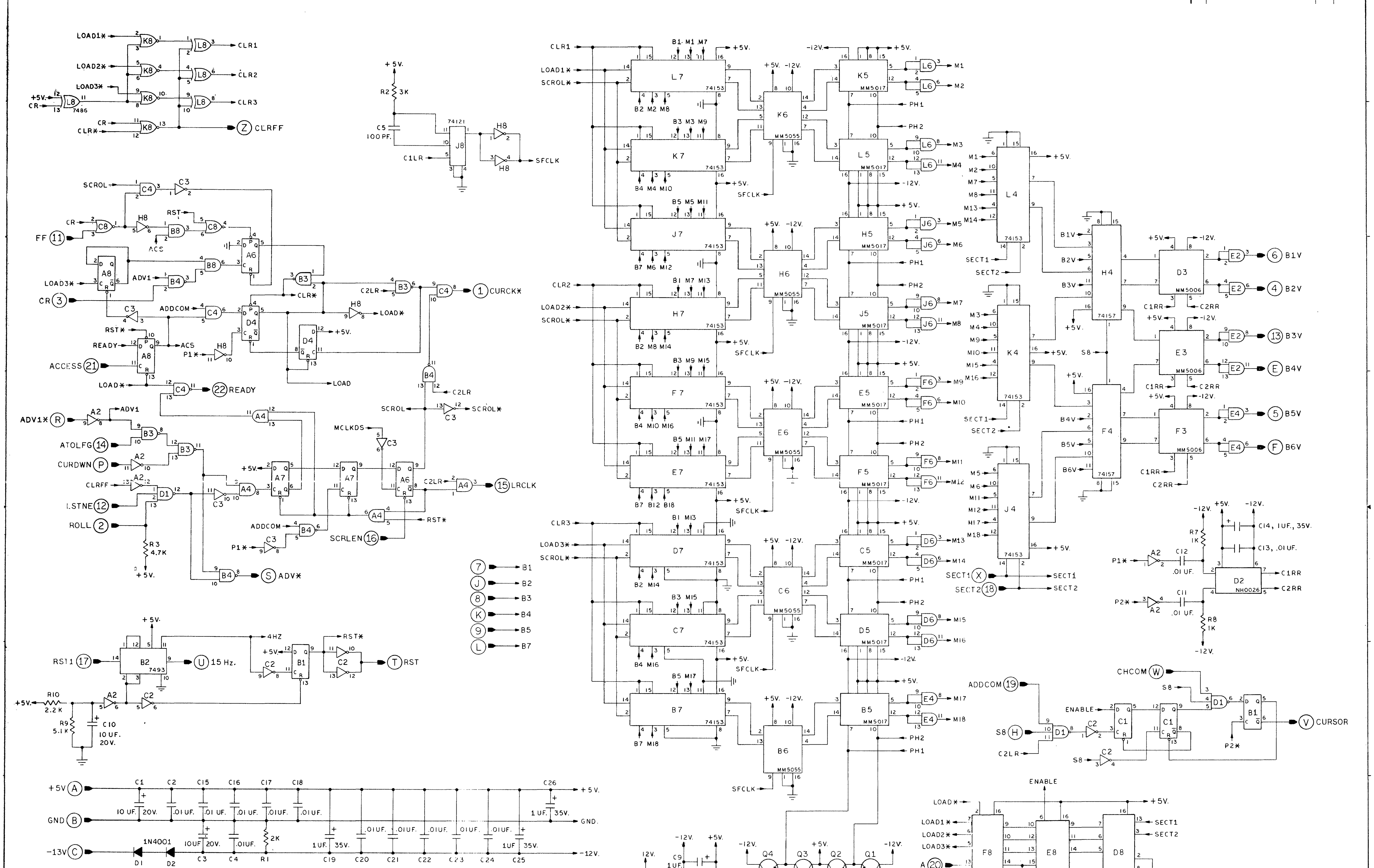
TOLERANCES: 1/64 FRAC, .005 DEC, 1 ANG
DO NOT SCALE DWG

DRAWN	Bologna	10/11/73
CHECKED	Coscolluela	10/17/73
ENG'R	Jacobs	10/17/73
APPROVED	Jacobs	10/17/73

ADDS Applied Digital Data System, Inc. Hauppauge, New York

ASSEMBLY
VG/GT

DWG NO 129-080 | SIZE D | SCALE — | SHEET 1 of 4 | REV —



I.C. TYPE	I.C. COORDINATES
SN7400	B3,4
SN7402	C8,K8
SN7404	A2,C2,3,H8
SN7408	A4,B8,C4,D6,E2,4,F6,J6,L6
SN7410	D1
SN7474	A6,7,8,B1,C1,D4
SN7485	E8
SN7486	L8
SN7493	B2
SN74121	J8
SN74153	B7,C7,D7,E7,F7,H7,J4,7,K4,7,L4,7
SN74155	D8,F8
SN74157	F4,H4

I.C. TYPE	I.C. COORDINATES
MM5006	D3,E3,F3
MM5017	B5,C5,D5,E5,F5,H5,J5,K5,L5
MM5055	B6,C6,E6,H6,K6
NH0026	A5,D2

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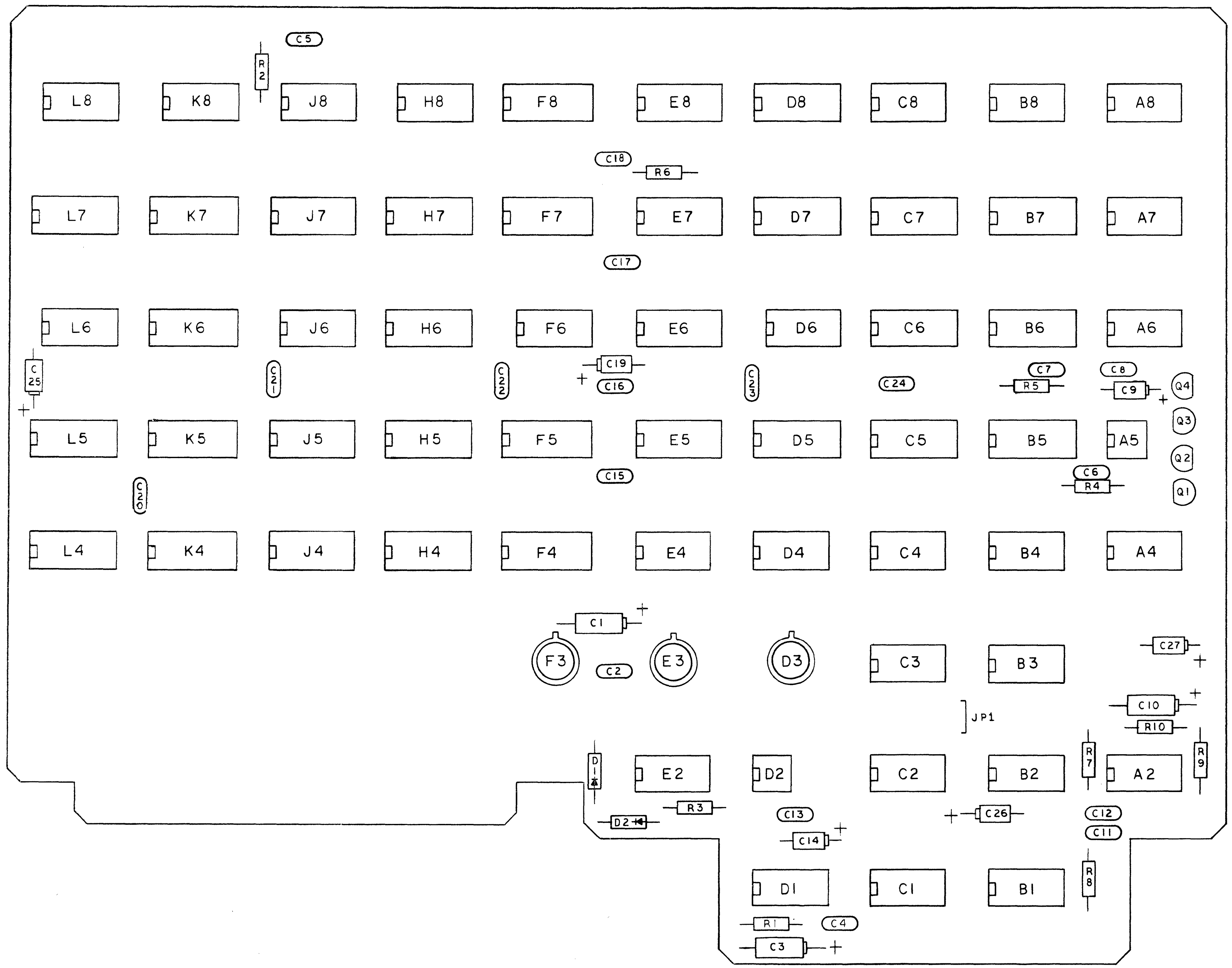
SCHEMATIC DIAGRAM
MC/GT

DWG NO 135-081 SIZE D SHEET 1 of 3

NEXT ASSY | USED ON | QTY

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



NOTE:
FOR BLINKING CURSOR INSTALL JP1.

10 – 25/26

NEXT ASSY	USED ON	QTY	

TOLERANCES:
1/64 FRAC .005 DEC 1 ANG
DO NOT SCALE DWG

DRAWN Bologna DATE 10/13/73
CHECKED
ENG'R
APPROVED

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ASSEMBLY
MC/GT

DWG NO 129-081 SIZE D SCALE — SHEET 1 of 3 REV

11. WIRELIST AND HARNESS LIST

This section contains two types of information:

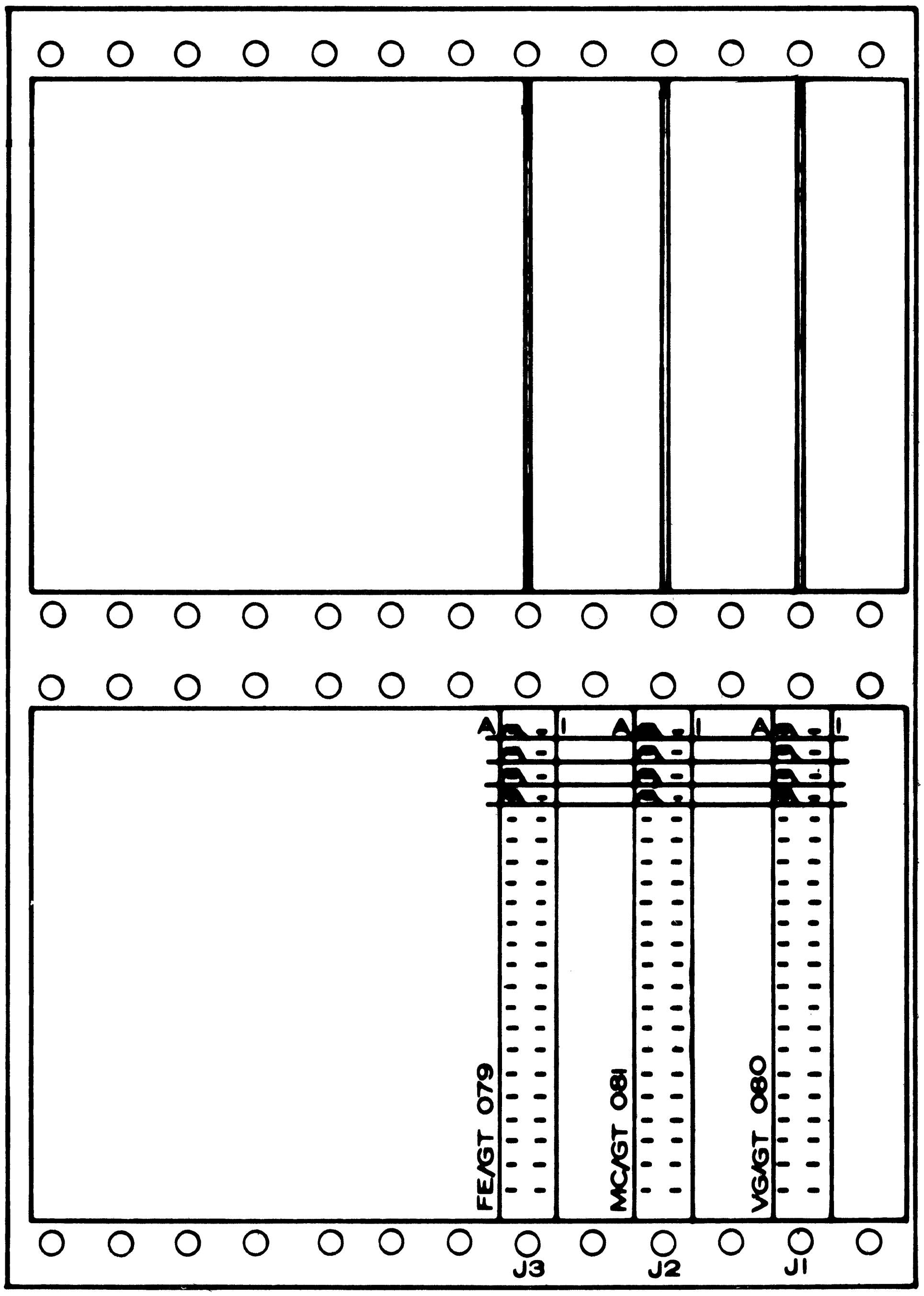
a) A point-to-point wire list of the 580 backplane wiring, with signal names.

b) A point-to-point wire list of the complete 580 harness, with appropriate signal names.

A drawing of the 580 card cage, as seen from the wirewrap side, is given in Figure 11.1 on the next page.

<u>580 BACK PLANE, WIRE WRAP SIDE</u>

Fig. 11·1



FRONT

WIRE WRAP LIST 580 - Page 1 of 2

VIDINT	J1, 1		J3, F
VIDEXT	J1, 2		J3, 5
P2*	J1, 3		J2, Y
HOME	J1, 4		J3, Z
LRCLK*	J1, 5		J2,15
CURSOR	J1, 6		J2, V
A	J1, 7		J2,20
ADV1*	J1, 8		J2, R
B3V	J1, 9		J2,13
B	J1,10		J2, N
B2V	J1,11		J2, 4
CURUP*	J1,12		J3, 8
SCRLEN	J1,13		J2,16
YLOAD*	J1,14		J3, K
LSTLNE	J1,15		J2,12
ADV*	J1,16		J2, S
RST1	J1,17		J2,17
VDRIVE	J1,18		J3,18
CURBK*	J1,19		J3, T
CURFR*	J1,20		J3, X
B2	J1,21	J2, J	J3, 3
B1	J1,22	J2, 7	J3, J
P1*	J1, E		J2,10
MCLKDS	J1, F		J2, M
S8	J1, H		J2, H
SECT2	J1, J		J2,18
B4V	J1, K		J2, E
B5V	J1, L		J2, 5
B6V	J1, M		J2, F
B1V	J1, N		J2, 6
CHOCM	J1, P		J2, W
ADDCOM	J1, R		J2,19
B7	J1, S	J2, L	J3, N

WIRE WRAP LIST 580 - Page 2 of 2

HDRIVE	J1, T		J3, W
SECT1	J1, U		J2, X
B5	J1, V	J2, 9	J3, 7
B6	J1, W		J3, R
B4	J1, X	J2, K	J3,13
B3	J1, Y	J2, 8	J3, E
XLOAD*	J1, Z		J3, 9
CURCK*	J2, 1		J3,20
ROLL	J2, 2		J3, 4
CR	J2, 3		J3,15
FF	J2,11		J3, S
ACCESS	J2,21		J3, L
CURDWN	J2, P		J3, Y
RST	J2, T		J3, P
15HZ	J2, U		J3, 6
CLRFF	J2, Z		J3,14
ATOLFG	J2,14		J3, H

From	To	
EIA, 25 Pin Female Connector	44 Pin, P1	SIGNAL NAME
1 } JUMPER	CHASSIS GND	GND
7 }	DAISY TO PIN 1	GND
2	P1,P	EIAOUT
3	P1,L	EIAIN
4	P1,W	RQSND
5	P1,18	CLSND
8	P1,12	CARDET
11	P1,V	SCA
12	P1,M	SCF
17	P1,9	LIN+
18	P1,K	LIN-
20	P1,8	DATTRY
22	P1,H	LBIAS
24	P1,11	LOUT+
25	P1,14	LOUT-

ENG'R	
DRAWN	
CHECKED	
APPROVED	

ADDS

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Hauppauge, New York

EIA CONNECTOR HARNESS

DWG NO 072-014 REV

SHEET 1 OF 1

From P1, 44 Pin Leaf	To	Signal Name
1	TB1,5	+5V
2	TB1,3	GND
3	TB1,7	-13V
4	TB1,6	+13V
5	SWITCH BRKT. TB2,5	AUTOLF
6	MONITOR CABLE, PIN K	VDRV
7	MONITOR CABLE, PIN F	HDRV
13	BAUD SW, S1, 5	FR1
15	BAUD SW, S1, 4	FR2
16	BAUD SW, S1, 3	FR3
17	PRINTER CONN, 1	PRTEIA
PIN B, FERRULE	PRINTER CONN, 2	GND
19	BAUD SW, S1, 2	FR4
20	BAUD SW, S1, 1	FR5
21	BAUD SW, S1, 6	FCOM
C	CONT. POT, PIN 1	VIDINT
PIN B, FERRULE	CONT. POT, PIN 3	GND
D	BNC	VIDEXT
PIN B, FERRULE	BND LUG	GND
E	TB2, 6	ROLL
J	TB2, 7	CARLT
U	TB2, 4	HDX
B	TO GROUND FERRULE (NOTE)	GND

NOTE: The Twisted Pair Ground (Black) and the 2 Coax Shields are tied together with one 18 gauge black wire in a Coax type ferrule. The drain wire goes to Pin B of P1. This is usually done while harnessing.

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN		
CHECKED		
APPROVED		POWER AND ACCESSORY HARNESS — DWG NO 072-011 — REV — SHEET 1 OF 1

FROM	TO	SIGNAL NAME
A.C. RECPT. 1	PWR SW, WIPER, 5	A.C. HOT
FUSE HOLDER	SW BRKT, WIPER, 2	A.C. FUSED
SW BRKT TB2,1	TB1,1	A.C. HOT, SWITCHED
SW BRKT TB2,2	TB1,2	A.C. FUSED, SWITCHED
SW BRKT TB2,1	CRT MOLEX, 1	A.C. HOT, SWITCHED
SW BRKT TB2,2	CRT MOLEX, 4	A.C. FUSED, SWITCHED
REAR PANEL A.C. GND	TB1,4	CHASSIS GND
REAR PANEL A.C. GND	A.C. RECPT.,2	CHASSIS GND
REAR PANEL A.C. GND	CRT MOLEX, 2	CHASSIS GND
TB1,4	SW BRKT LUG	CHASSIS GND
A.C. RECPT. 3	FUSE BRKT, SIDE LUG	
TB1,7	SW BRKT TB2,8	-13V
P1,A	SONALERT (-)	ALARM*
TB1,6	SONALERT (+)	+13V

ENG'R		
DRAWN		
CHECKED		
APPROVED		

ADDS

Applied Digital Data Systems, Inc.
Hauppauge, New York

BASIC HARNESS

DWG NO 072-010 REV

SHEET 1 OF 1

From / To

KEYBRD, 30 PIN	TB1 & 44 PIN, P1	SIGNAL NAME
1	TB1,3	GND
2	TB1,5	+5V
6	P1,10	BREKEY
9	P1,T	REPEAT
J	P1,F	KBSTB
K	P1,N	B7KB
L	P1,S	B6KB
M	P1,R	B5KB
N	P1,22	B4KB
P	P1,Z	B3KB
R	P1,Y	B2KB
S	P1,X	B1KB

Note:

Install Dummy Pins on 30 Pin side into Pins A,D, 12 and 15.

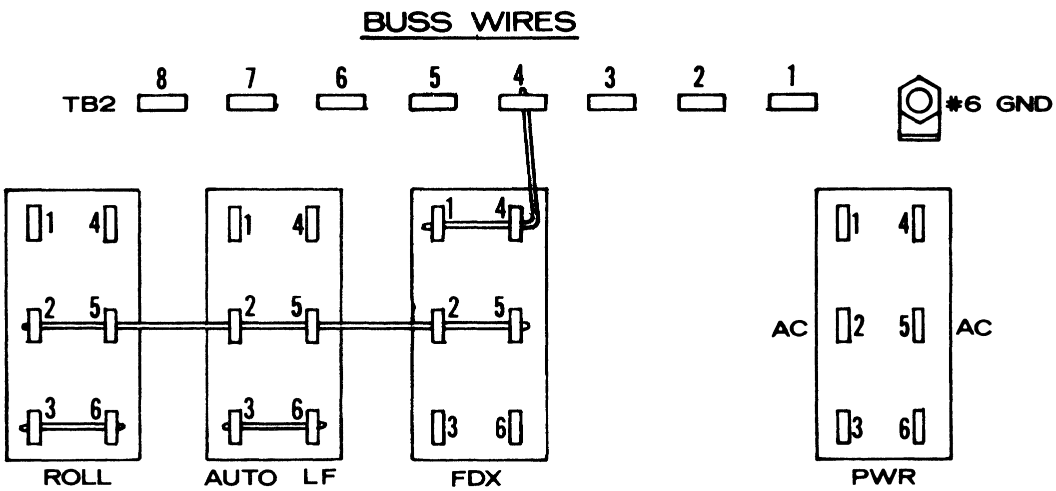
ENG'R		ADDS — Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN		
CHECKED		KEYBOARD HARNESS — DWG NO 072-015 — REV
APPROVED		SHEET 1 OF 1

From	To	
MONITOR, 10 Pin Leaf	BRITE, CONT. POTS	SIGNAL NAME
A (SAME LEAF)	GND LUG	GND
A	JUMP TO PIN E	
B	"BRITE" PIN 1	+BRT
C	"BRITE" PIN 3	-BRT
D	"BRITE" PIN 2	WIPER
J	"CONT." PIN 2	
L	"CONT." PIN 3	SHIELD

1 DUMMY PINS FOR CONTACT PRESSURE

5 PUT 22 BUS IN LEAF, THEN CUT.

ENG'R		**ADDS** Applied Digital Data Systems, Inc. Hauppauge, New York	
DRAWN			
CHECKED		MONITOR HARNESS	DWG NO 072-012 REV
APPROVED			SHEET 1 OF 1



From	To	Signal Name
PWR,1	TB2,2	AC
PWR,4	TB2,1	AC
ROLL, 6	TB2,1	
AUTOLF, 6	TB2,5	
FDX,5	GND LUG	
AMBER BULB	TB2,8	PRE WIRED TO ASSEMBLY
AMBER BULB	TB2,7	PRE WIRED TO ASSEMBLY
RED BULB	TB2,1	PRE WIRED TO ASSEMBLY
RED BULB	TB2,2	PRE WIRED TO ASSEMBLY

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN		
CHECKED		SWITCH BRACKET HARNESS
APPROVED		DWG NO 072-013 REV; SHEET 1 OF 1