CONTROL DATA CORPORATION

CONTROL DATA®
1700 COMPUTER SYSTEM

CODES

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1700 COMPUTER SYSTEM

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RECORD of REVISIONS

REVISION	NOTES
A	Original printing.
(4-4-66)	
B	PCO 16001 adds information for the 1718-A Satellite
(3-15-67)	Coupler, 1731-A/B Magnetic Tape Controllers, and
	1738-A/B Disk Pack Controller. This edition obsoletes
	all previous editions.
C	Engineering Change Order 20275. This edition
(8-12-68)	obsoletes all previous editions.
D	Manual Revised; includes Engineering Change Order
(2-6-70)	23214. Pages 21, 22, and 23 revised.
E	Manual revised; includes Engineering Change Order
(2-6-70)	24531. Pages 13, 14, 15, 51, 52, and 53 added. This
	edition obsoletes all previous editions.
F	Manual revised; includes Engineering Change Order
(8-1-72)	30429. Pages 20 and 28 are revised.
G	Manual revised; Engineering Change Order 33738. Pages
(5-9-73)	iii, 50, and 52 are revised. Pages 41.1, 41.2, 41.3,
	46.1, 46.2, 46.3, 46.4 are added.
H	Manual revised and updated to incorporate ECO DS17019.
(10-74)	

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Address comments concerning manual to:
Control Data Corporation
Technical Publications Department
4455 Eastgate Mall
La Jolla, California 92037

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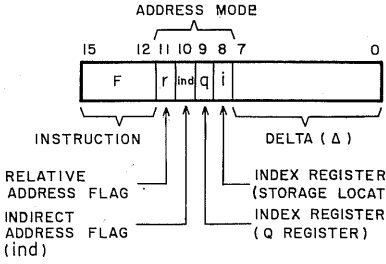
INSTRUCTIONS

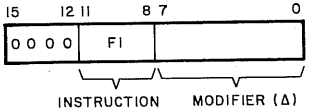
STORAGE REFERENCE



F			
1	0001	JMP	Jump
2	0010	MUI	Multiply Integer
3	0011	DVI	Divide Integer
4	0100	STQ	Store Q
5	0101	RTJ	Return Jump
6	0110	STA	Store A
7	0111	SPA	Store A, Parity to A
8	1000	ADD	Add A
9	1001	SUB	Subtract
A	1010	AND	AND With A
B	1011	EOR	Exclusive OR With A
C	1100	LDA	Load A
D	1101	RAO	Replace Add 1 in Storage
E	1110	LDQ	Load Q
F	1111	ADQ	Add Q

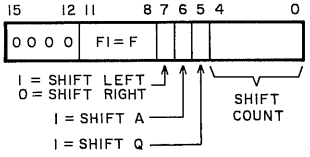
REGISTER REFERENCE/SHIFT

REGISTER REFERENCE

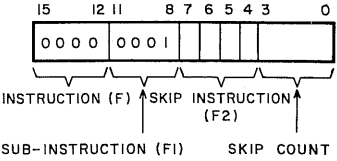


F1			
0	0000	SLS	Selective Stop
1	0001		SKIPS
2	0010	INP	Input to A
3	0011	OUT	Output From A
4	0100	EIN	Enable Interrupt
5	0101	IIN	Inhibit Interrupt
6	0110	SPB	Set Program Protect
7	0111	CPB	Clear Program Protect
8	1000		INTERREGISTER
9	1001	INA	Increase A
A	1010	ENA	Enter A
B	1011	NOP	No Operation
C	1100	ENQ	Enter Q
D	1101	INQ	Increase Q
E	1110	EXI	Exit Interrupt State
F	1111		SHIFTS

SHIFT

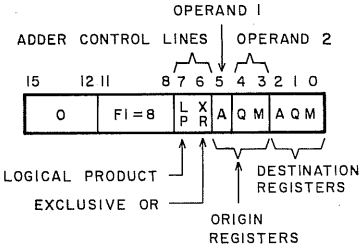


SKIP



F2			
0	0000	SAZ	A = +0
1	0001	SAN	A ≠ +0
2	0010	SAP	A = +
3	0011	SAM	A = -
4	0100	SQZ	Q = +0
5	0101	SQN	Q ≠ +0
6	0110	SQP	Q = +
7	0111	SQM	Q = -
8	1000	SWS	Skip If Switch Set
9	1001	SWN	Skip If Switch Not Set
A	1010	SOV	Skip On Overflow
B	1011	SNO	Skip On No Overflow
C	1100	SPE	Skip On Storage Parity Error
D	1101	SNP	Skip On No Storage Parity Error
E	1110	SPF	Skip On Program Protect Fault
F	1111	SNF	Skip On No Program Protect Fault

INTERREGISTER



INTERREGISTER LOGICAL OPERATIONS

LP (Bit 7)	XR (Bit 6)	Logical Operations
0	0	Arithmetic Sum
0	1	Exclusive OR
1	0	Logical Product
1	1	Complement Logical Product

OPERAND 1

A (Bit 5)	Operand 1
0	FFFF
1	Contents of A

OPERAND 2

Q (Bit 4)	M (Bit 3)	Operand 2
0	0	FFFF
0	1	Contents of M (Mask register)
1	0	Contents of Q
1	1	Inclusive OR of (Q) and (M)

Inclusive OR Truth Table

Q. Reg. Bit	M Reg. Bit	Inclusive OR
0	0	0
1	0	1
0	1	1
1	1	1

DESTINATION REGISTERS

A (Bit 2)	Q (Bit 1)	M (Bit 0)	Destination Register
0	0	0	See note b.
0	0	1	M (Mask register)
0	1	0	Q
1	0	0	A
0	1	1	M and Q
1	0	1	M and A
1	1	0	Q and A
1	1	1	M, Q, and A

INTERREGISTER INSTRUCTION TRUTH TABLE

Operand 1	Operand 2	Exclusive OR	Logical Product	Complement Logical Product
0	0	0	0	1
0	1	1	0	1
1	0	1	0	1
1	1	0	1	0

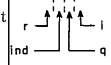
Notes:

a. Register transfers can be accomplished by setting LP and XR to "0" and either operand 1 or operand 2 to $FFFF_{16}$.

b. Magnitude comparisons without destroying either operand can be done by setting LP and XR to "0", selecting no destination register, and then testing the OVERFLOW indicator.

c. Complementing registers can be done by setting LP to "0", XR to "1", and either operand 1 or operand 2 to $FFFF_{16}$.

STORAGE ADDRESSING RELATIONSHIPS

Mode	Address Mode Bits Binary	Hex	Delta
Absolute	0000	0	$\Delta \neq 0$
Constant			$\Delta = 0$
Absolute	0001	1	$\Delta \neq 0$
Constant			$\Delta = 0$
Absolute	0010	2	$\Delta \neq 0$
Constant			$\Delta = 0$
Absolute	0011	3	$\Delta \neq 0$
Constant			$\Delta = 0$
Indirect	0100	4	$\Delta \neq 0$
Storage			$\Delta = 0$
Indirect	0101	5	$\Delta \neq 0$
Storage			$\Delta = 0$
Indirect	0110	6	$\Delta \neq 0$
Storage			$\Delta = 0$
Indirect	0111	7	$\Delta \neq 0$
Storage			$\Delta = 0$
Relative	1000	8	$\Delta \neq 0$
16-Bit Relative			$\Delta = 0$
Relative	1001	9	$\Delta \neq 0$
16-Bit Relative			$\Delta = 0$
Relative	1010	A	$\Delta \neq 0$
16-Bit Relative			$\Delta = 0$
Relative	1011	B	$\Delta \neq 0$
16-Bit Relative			$\Delta = 0$
Relative Indirect	1100	C	$\Delta \neq 0$
Relative Indirect			$\Delta = 0$
Relative Indirect	1101	D	$\Delta \neq 0$
Relative Indirect			$\Delta = 0$
Relative Indirect	1110	E	$\Delta \neq 0$
Relative Indirect			$\Delta = 0$
Relative Indirect	1111	F	$\Delta \neq 0$
Relative Indirect			$\Delta = 0$

Effective Address	Address of Next Instruction
Δ	P + 1
P + 1	P + 2
Δ + (00FF)	P + 1
(P + 1) + (00FF)*	P + 2
Δ + (Q)	P + 1
(P + 1) + (Q)*	P + 2
Δ + (Q) + (00FF)	P + 1
(P + 1) + (Q) + (00FF)*	P + 2
(Δ)	P + 1
(P + 1)	P + 2
(Δ) + (00FF)	P + 1
(P + 1) + (00FF)	P + 2
(Δ) + (Q)	P + 1
(P + 1) + (Q)	P + 2
(Δ) + (Q) + (00FF)	P + 1
(P + 1) + (Q) + (00FF)	P + 2
P + Δ	P + 1
P + 1 + (P + 1)	P + 2
P + Δ + (00FF)	P + 1
P + 1 + (P + 1) + (00FF)	P + 2
P + Δ + (Q)	P + 1
P + 1 + (P + 1) + (Q)	P + 2
P + Δ + (Q) + (00FF)	P + 1
P + 1 + (P + 1) + (Q) + (00FF)	P + 2
(P + Δ)	P + 1
[P + 1 + (P + 1)]	P + 2
(P + Δ) + (00FF)	P + 1
[P + 1 + (P + 1)] + (00FF)	P + 2
(P + Δ) + (Q)	P + 1
[P + 1 + (P + 1)] + (Q)	P + 2
(P + Δ) + (Q) + (00FF)	P + 1
[P + 1 + (P + 1)] + (Q) + (00FF)	P + 2

*Effective address is the operand for read-operand-type instructions

INSTRUCTION EXECUTION TIMES

		Execution Time (usec)
AAB	Transfer Arithmetic Sum A, Q + M	1.1
AAM	Transfer Arithmetic Sum A, M	1.1
AAQ	Transfer Arithmetic Sum A, Q	1.1
ADD	Add A	2.2
ADQ	Add Q	2.2
ALS	A Left Shift	$1.1 + \left(\frac{\text{shift count}}{2}\right)(.2)$
AND	AND With A	2.2
ARS	A Right Shift	$1.1 + \left(\frac{\text{shift count}}{2}\right)(.2)$
CAB	Transfer Complement Logical Product A, Q + M	1.1
CAM	Transfer Complement Logical Product A, M	1.1
CAQ	Transfer Complement Logical Product A, Q	1.1
CLR	Clear To Zero	1.1
CPB	Clear Program Protect	2.2
DVI	Divide Integer	9.0
EAB	Transfer Exclusive OR A, Q + M	1.1
EAM	Transfer Exclusive OR A, M	1.1
EAQ	Transfer Exclusive OR A, Q	1.1
EIN	Enable Interrupt	1.1
ENA	Enter A	1.1
ENQ	Enter Q	1.1
EOR	Exclusive OR With A	2.2
EXI	Exit Interrupt State	2.2
IIN	Inhibit Interrupt	1.1
INA	Increase A	1.1
INP	Input to A	1.1 min., 10 max
INQ	Increase Q	1.1
JMP	Jump	1.1
LAB	Transfer Logical Product A, Q + M	1.1
LAM	Transfer Logical Product A, M	1.1

		Execution Time (usec)
LAQ	Transfer Logical Product A, Q	1.1
LDA	Load A	2.2
LDQ	Load Q	2.2
LLS	Long Left Shift	1.1 + (shift count) (.2)
LRS	Long Right Shift	1.1 + (shift count) (.2)
MUI	Multiply Integer	7.0
NOP	No Operation	1.1
OUT	Output From A	$\overline{1.1}$ min., 10 max.
QLS	Q Left Shift	$1.1 + \left(\frac{\text{shift count}}{2}\right)$ (.2)
QRS	Q Right Shift	$1.1 + \left(\frac{\text{shift count}}{2}\right)$ (.2)
RAO	Replace Add 1 in Storage	3.3
RTJ	Return Jump	2.2
SAM	Skip If A = -	1.1
SAN	Skip if A ≠ +0	1.1
SAP	Skip if A = +	1.1
SAZ	Skip If A = +0	1.1
SET	Set to Ones	1.1
SLS	Selective Stop	1.1
SNF	Skip On No Program Protect Fault	1.1
SNO	Skip On No Overflow	1.1
SNP	Skip On No Storage Parity Error	1.1
SOV	Skip On Overflow	1.1
SPA	Store A, Parity to A	2.2
SPB	Set Program Protect	2.2
SPE	Skip On Storage Parity Error	1.1
SPF	Skip On Program Protect Fault	1.1
SQM	Skip If Q = -	1.1
SQN	Skip If Q ≠ +0	1.1
SQP	Skip If Q = +	1.1
SQZ	Skip If Q = +0	1.1
STA	Store A	2.2
STQ	Store Q	2.2

		Execution Time (usec)
SUB	Subtract	2.2
SWN	Skip If Switch Not Set	1.1
SWS	Skip If Switch Set	1.1
TCA	Transfer Complement A	1.1
TCB	Transfer Complement Q + M	1.1
TCM	Transfer Complement M	1.1
TCQ	Transfer Complement Q	1.1
TRA	Transfer A	1.1
TRB	Transfer Q + M	1.1
TRM	Transfer M	1.1
TRQ	Transfer Q	1.1

Note: Add 1.1 microsecond if Storage Index Register is used.

Add 1.1 microsecond for each level of Indirect Addressing.

1774 INSTRUCTION EXECUTION TIMES

		Execution Time (μsec)
AAB	Transfer Arithmetic Sum A, Q+M	1.5
AAM	Transfer Arithmetic Sum A, M	1.5
AAQ	Transfer Arithmetic Sum A, Q	1.5
ADD	Add A	3.0
ADQ	Add Q	3.0
ALS	A Left Shift 1.5+(shift count)	(.5)
AND	AND With A	3.0
ARS	A Right Shift 1.5+(shift count)	(.5)
CAB	Transfer Complement Logical Product A, Q, + M	1.5
CAM	Transfer Complement Logical Product A, M	1.5
CAQ	Transfer Complement Logical Product A, Q	1.5
CLR	Clear To Zero	1.5
CPB	Clear Program Protect	3.5
DCA	Disable Character Addressing	1.5
DVI	Divide Integer	30.0
EAB	Transfer Exclusive OR A, Q, M	1.5
EAM	Transfer Exclusive OR A, M	1.5
EAQ	Transfer Exclusive OR A, Q	1.5
ECA	Enable Character Addressing	1.5
EIN	Enable Interrupt	1.5
ENA	Enter A	1.5
ENQ	Enter Q	1.5
EOR	Exclusive OR With A	3.0
EXI	Exit Interrupt State	3.5
IIN	Inhibit Interrupt	1.5

INA	Increase A	1.5
INP	Input to A	2.0 min., 10 max.
INQ	Increase Q	1.5
JMP	Jump	1.5
LAB	Transfer Logical Product A, Q+M	1.5
LAM	Transfer Logical Product A, M	1.5
LAQ	Transfer Logical Product A, Q	1.5
LDA	Load A	3.0
LDQ	Load Q	3.0
LLS	Long Left Shift 1.5+(shift count)	(1.0)
LRS	Long Right Shift 1.5+(shift count)	(1.0)
MUI	Multiply Integer	20.0
NOP	No Operation	1.5
OUT	Output From A	2.0 min., 10 max.
GLS	Q Left Shift 1.5+(shift count)	(.5)
QRS	Q Right Shift 1.5+(shift count)	(.5)
RAO	Replace Add 1 in Storage	4.5
RTJ	Return Jump	3.5
SAM	Skip If A = -	2.0
SAN	Skip if A ≠ +0	2.0
SAP	Skip if A = +	2.0
SAZ	Skip if A = +0	2.0
SET	Set to Ones	1.5
SLS	Selective Stop	1.5
SNF	Skip On No Program Protect Fault	2.0
SNO	Skip On No Overflow	2.0
SNP	Skip On No Storage Parity Error	2.0
SOV	Skip On Overflow	2.0
SPA	Store A, Parity to A	3.0
SPB	Set Program Protect	3.5
SPE	Skip On Storage Parity Error	2.0
SPF	Skip on Program Protect Fault	2.0
SQM	Skip if Q = -	2.0
SQN	Skip if Q ≠ +0	2.0
SQP	Skip if Q = +	2.0
SQZ	Skip if Q = +0	2.0

STA	Store A	3.0
STQ	Store Q	3.0
SUB	Subtract	3.0
SWN	Skip If Switch Not Set	2.0
SWS	Skip If Switch Set	2.0
TCA	Transfer Complement A	1.5
TCB	Transfer Complement Q + M	1.5
TCM	Transfer Complement M	1.5
TCQ	Transfer Complement Q	1.5
TRA	Transfer A	1.5
TRB	Transfer Q + M	1.5
TRM	Transfer M	1.5
TRQ	Transfer Q	1.5

Note: Add 0.75 microsecond if Storage Index Register is used.

Add 1.5 microsecond for each level of Indirect Addressing

Add 0.5 microsecond for Q indexing

1784-1/2 INSTRUCTION EXECUTION TIMES

		Execution Time (μsec) 1784-1	1784-2
AAB	Transfer Arithmetic Sum A, Q+M	0.900	0.600
AAM	Transfer Arithmetic Sum A, M	0.900	0.600
AAQ	Transfer Arithmetic Sum A, Q	0.900	0.600
ADD	Add A	1.800	1.200
ADQ	Add Q	1.800	1.200
	SHIFTS		
ALS QLS	A Left Shift \ If N is Q Left Shift / Even*	$0.900 + \frac{N}{2}(0.818)$	$0.600 + \frac{N}{2}(0.546)$
ARS QRS	A Right Shift \ If N Is Q Right Shift / Odd	$0.900 + \frac{(N+1)}{2}(0.818)$	$0.600 + \frac{(N+1)}{2}(0.546)$
LRS LLS	Long Right Shift Long Left Shift	$0.900 + N(0.818)$	$0.600 + N(0.546)$
AND	AND with A	1.800	1.200
CAB	Transfer Complement Logical Product A, Q+M	0.900	0.600
CAM	Transfer Complement Logical Product A, M	0.900	0.600
CAQ	Transfer Complement Logical Product A, Q	0.900	0.600
CLR	Clear to Zero	0.900	0.600
CPB	Clear Program Protect	2.700	1.800

*N = Shift Count
Any shift of 0 places or a short shift of one place takes 0.900 microsecond (1784-1) or 0.600 microsecond (1784-2). Add 0.273 if short shift count is odd and greater than 1.

DVI	Divide Integer		17.344	11.563
EAB	Transfer Exclusive OR of A, Q+M		0.900	0.600
EAM	Transfer Exclusive OR of A, M		0.900	0.600
EAQ	Transfer Exclusive OR of A, Q		0.900	0.600
EIN	Enable Interrupt		0.900	0.600
ENA	Enter A		0.900	0.600
ENQ	Enter Q		0.900	0.600
EOR	Exclusive OR with A		1.800	1.200
EXI	Exit Interrupt State		2.209	1.473
IIN	Inhibit Interrupt		0.900	0.600
INA	Increase A		0.900	0.600
INP	Input to A	Minimum Maximum	2.268 9.000	1.512 6.000
INQ	Increase Q		0.900	0.600
JMP	Jump		0.900	0.600
LAB	Transfer Logical Product A, Q+M		0.900	0.600
LAM	Transfer Logical Product A, M		0.900	0.600
LAQ	Transfer Logical Product A, Q		0.900	0.600
LDA	Load A		1.800	1.200
LDQ	Load Q		1.800	1.200
MUI	Multiply Integer		17.344	11.563
NOP	No Operation		0.900	0.600
OUT	Output from A	Minimum Maximum	2.268 9.000	1.512 6.000
RAO	Replace Add One in Storage		2.700	1.800
RTJ	Return Jump		1.800	1.200
SAM	Skip if A = -		1.309	0.873
SAN	Skip if A ≠ +0		1.309	0.873
SAP	Skip if A = +		1.309	0.873
SAZ	Skip if A = +0		1.309	0.873
SET	Set to Ones		0.900	0.600
SLS	Selective Stop		0.900	0.600
SNF	Skip on No Program Protect Fault		1.309	0.873

SNO	Skip on No Overflow	1.309	0.873
SNP	Skip on No Storage Parity Error	1.309	0.873
SOV	Skip on Overflow	1.309	0.873
SPA	Store A, Parity to A	1.800	1.200
SPB	Set Program Protect	2.700	1.800
SPE	Skip on Storage Parity Error	1.309	0.873
SPF	Skip on Program Protect Fault	1.309	0.873
SQM	Skip if Q = -	1.309	0.873
SQN	Skip if Q ≠ +0	1.309	0.873
SQP	Skip if Q = +	1.309	0.873
SQZ	Skip if Q = +0	1.309	0.873
STA	Store A	1.800	1.200
STQ	Store Q	1.800	1.200
SUB	Subtract	1.800	1.200
SWN	Skip if Switch not Set	1.309	0.873
SWS	Skip if Switch Set	1.309	0.873
TCA	Transfer Complement A	0.900	0.600
TCB	Transfer Complement Q+M	0.900	0.600
TCM	Transfer Complement M	0.900	0.600
TCQ	Transfer Complement Q	0.900	0.600
TRA	Transfer A	0.900	0.600
TRB	Transfer Q+M	0.900	0.600
TRM	Transfer M	0.900	0.600
TRQ	Transfer Q	0.900	0.600

Notes:
1. Add 0.409 microsecond (1784-1) or 0.273 microsecond (1784-2) for all storage reference instructions whose address is relative with Q indexing.
2. Add 0.900 microsecond (1784-1) or 0.600 microsecond (1784-2) for each level of indirect address.
3. Subtract 0.490 microsecond (1784-1) or 0.723 microsecond (1784-2) when the operand is immediate.
4. Add 0.900 microsecond (1784-1) or 0.600 microsecond (1784-2) if storage indexing is used.

5. Instructions causing protect system violations are executed as unprotected selected stops, taking 1.227 microseconds (1784-1) or 0.818 microsecond (1784-2).
6. The dynamic MOS memory cells require refreshing cycles to maintain the memory contents. In the 1784-1, a refresh cycle of 0.735 microsecond will occur every 48 microseconds. In the 1784-2, a refresh cycle of 0.490 microsecond will occur every 32 microseconds.
7. Memory refresh cycles take priority over direct storage accesses, which in turn have priority over CPU accesses to memory.
8. Execution times are given for both the 1784-1, with a memory cycle time of 900 nanoseconds, and the 1784-2, with a memory cycle time of 600 nanoseconds.

INTERRUPT STATE DEFINITIONS

	Interrupt state$_{10}$	Value of Δ to exit state$_{16}$	Location of return address$_{16}$	Location of first instruction after interrupt occurs$_{16}$
*	00	00	0100	0101
*	01	04	0104	0105
	02	08	0108	0109
	03	0C	010C	010D
	04	10	0110	0111
	05	14	0114	0115
	06	18	0118	0119
	07	1C	011C	011D
**	08	20	0120	0121
	09	24	0124	0125
	10	28	0128	0129
	11	2C	012C	012D
	12	30	0130	0131
	13	34	0134	0135
	14	38	0138	0139
	15	3C	013C	013D

*Interrupts in basic computer

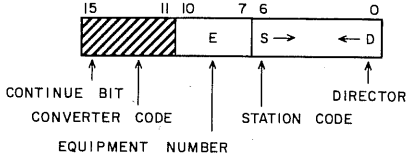
**Interrupts added by 1705 Interrupt Data Channel option

INPUT/OUTPUT

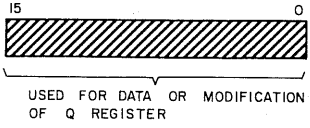
AQ CHANNEL PERIPHERAL DEVICE ADDRESSING

ADDRESSES

Q Register

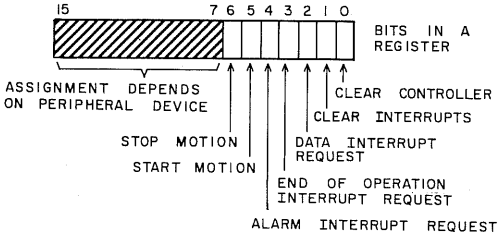


A Register



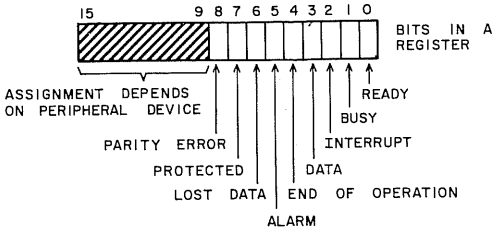
OPERATIONS

Director Function



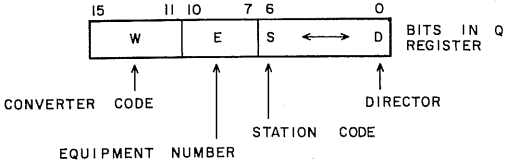
STATUS RESPONSE

Director Status



1706-A BUFFERED DATA CHANNEL

ADDRESSES



W*			Computer Instruction	
1706 #3	1706 #2	1706 #1	Input	Output
0C	07	02	Direct input	Direct output
0D	08	03	Terminate buffer: 1706 current address**	Function
0E	09	04	1706 status	Buffered output
0F	0A	05	1706 current address	Buffered input

*The left digit is binary; the right digit is hexadecimal.

**Terminate buffer operation will cause the 1706 to remain busy for 10 μsec.

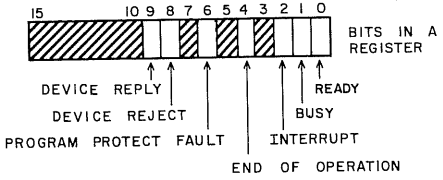
OPERATIONS

Function

Bit in A Register		Meaning
A15	= 1	Set condition for "1's" in bits A14 - A00
	= 0	Clear condition for "1's" in bits A14 - A00
A14 - A01		Not defined
A00		Enable interrupt on 1706 end of operation.

STATUS RESPONSE

1706 Status

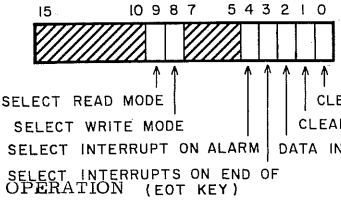


ADDRESSES

Q Register	Computer Instruction	
	Output From A	Input To A
0090	Write	Read
0091	Director Function	Director Status

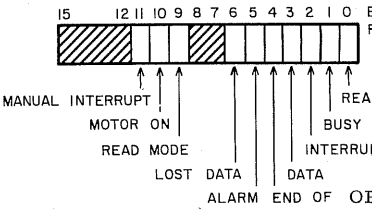
OPERATIONS

Director Function



STATUS RESPONSE

Director Status

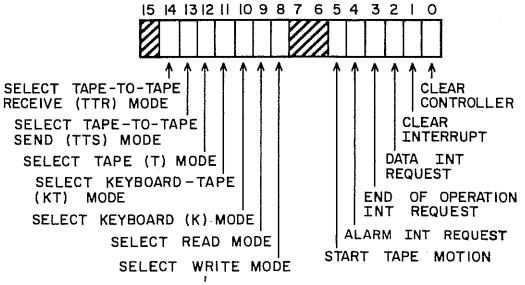


ADDRESSES

Same as for 1711/1712 Teletypewriter.

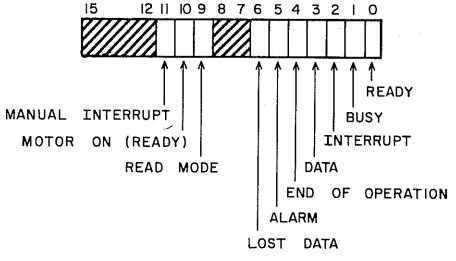
OPERATIONS

Director Function



STATUS RESPONSE

Director Status



1711-4/5/1713-4/5 TELETYPEWRITER AND CDT (CONVERSATIONAL DISPLAY TERMINAL)

ADDRESSES

Same as for the 1711/1712 Teletypewriter.

OPERATIONS

Same as for the 1711/1712 Teletypewriter with the addition of bit 10 and bit 13 in the register:

Bit 10 = Reconnect printer
Bit 13 = Disconnect printer

STATUS RESPONSE

Same as for the 1711/1712 Teletypewriter with the following exceptions:

Bit 0 = Not used; always set to 1
Bit 7 = Parity error
Bit 10 = Not used

1711/1712/1713 CODING

Control Characters:

NUL	Null (two successive nulls lock keyboard and stop tape reader)
EOA	End of Address (cc)*
EOT	End of Transmission, shuts off motors (cc)
WRU	Who are you? (cc)
BELL	Bell (audible or attention signal)
TAB	Horizontal Tab (FE)
LINE FEED	Line Feed (FE)
VT	Vertical Tab (FE)
FORM	Form, top of page (FE)
RETURN	Carriage Return, does not advance paper (FE)
TAPE	Tape (no operation)
X-OFF	Auxiliary off (no operation)
~~TAPE~~	Not Tape (no operation)
RUB OUT	Delete (punches all levels on paper tape, no effect on printer)

*(cc) Communication Control
(FE) Format Effector

Graphic Characters:

Column/Row	Symbol	Name
2/0	SP	Space (normally non-printing)
2/1	!	Exclamation Point
2/2	"	Quotation Marks (Diaeresis)
2/3	#	Number Sign
2/4	$	Dollar Sign
2/5	%	Percent
2/6	&	Ampersand
2/7	'	Apostrophe (Closing Single Quotation Mark; Acute Accent)
2/8	(	Opening Parenthesis
2/9	)	Closing Parenthesis
2/10	*	Asterisk
2/11	+	Plus
2/12	,	Comma (Cedilla)
2/13	-	Hyphen (Minus)
2/14	.	Period (Decimal Point)
2/15	/	Slant
3/10	:	Colon
3/11	;	Semicolon
3/12	<	Less Than
3/13	=	Equals
3/14	>	Greater Than
3/15	?	Question Mark
4/0	@	Commercial Art
5/11	[	Opening Bracket
5/12		Grave Accent (Opening) Single Quotation Mark)
5/13	]	Closing Bracket
5/14	↑	*
5/15	←	*
7/11	{	* Opening Brace
7/13	}	* Closing Brace

* See Table page 34

** Optional Braces replace Brackets. Both use the same type pallet position in the type box.

b7 → b6 → b5 → BITS	b4 ↓	b3 ↓	b2 ↓	b1 ↓	COLUMN → ROW ↓	0 0 0 0
	0	0	0	0	0	NUL
	0	0	0	1	1	Note 1
	0	0	1	0	2	*EOA
	0	0	1	1	3	
	0	1	0	0	4	EOT
	0	1	0	1	5	*WRU
	0	1	1	0	6	*RU
	0	1	1	1	7	BELL
	1	0	0	0	8	
	1	0	0	1	9	TAB
	1	0	1	0	10	LINE FEED
	1	0	1	1	11	VT
	1	1	0	0	12	FORM
	1	1	0	1	13	RETURN
	1	1	1	0	14	
	1	1	1	1	15	

*May be generated from keyboard but does not affect printer; it is punched on tape.

Note 1 Any character left blank does not affect the printer but is punched on tape.

$0\ 0\ 1$	$0\ 1\ 0$	$0\ 1\ 1$	$1\ 0\ 0$	$1\ 0\ 1$	$1\ 1\ 0$	$1\ 1\ 1$
1	2	3	4	5	6	7
	SP	0	@	P		
	!	1	A	Q		
*TAPE	"	2	B	R		
*X-OFF	#	3	C	S		
*~~TAPE~~	$	4	D	T		
	%	5	E	U		
	&	6	F	V		
	'	7	G	W		
	(	8	H	X		
	)	9	I	Y		
	*	:	J	Z		
	+	;	K	[		{
	,	<	L	\		
	-	=	M	]		}
	.	>	N	↑		
	/	?	O	←		*RUB OUT

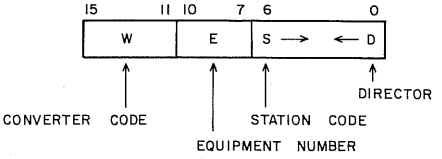
* The 1711-1, 1712 and 1713-1 use ASCII63 codes. The 1711-2 and 1713-2 use ASCII68 codes. The following table shows the equivalent characters where differences exist for ASCII63 and ASCII68.

** Optional Braces replace Brackets. Both use the same type pallet position in the type box.

COLUMN/ROW	ASCII63	ASCII68
2/2	"	Modified to afford multiple usage as quotation or diaress
2/7	'	Slight tilt affording multiple usage as apostrophy or acute accent.
2/12	,	Modified to afford multiple usage as comma or cedilla.
3/0	0	Slimmer zero
4/15	o	Fatter "O"
5/14	↑	^(circumflex)
5/15	←	_(underline)

1716-A COUPLING DATA CHANNEL

ADDRESSES



W*			Computer Instruction	
1716 #3	1716 #2	1716 #1	Input To A	Output From A
0B	06	01		Buffered transfer
0C	07	02	Direct input	Direct output
0D	08	03**	Terminate buffer 1716 current address	Function
0E	09	04	1716 status	Buffered output
0F	0A	05	1716 current address	Buffered input

*The left digit is binary; the right digit is hexadecimal.

**Terminate buffer operation will cause the 1706 to remain busy for 10 μsec.

OPERATIONS

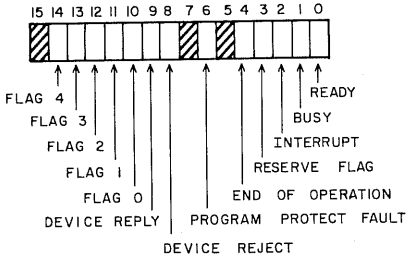
Functions

Bit in A Register	Meaning
A15 = 1	Set condition for "1's" in bits A14 - A00
A15 = 0	Clear condition for "1's" in bits A14-A00
A14	Flag 4
A13	Flag 3
A12	Flag 2
A11	Flag 1
A10	Flag 0
A09	Mask 4

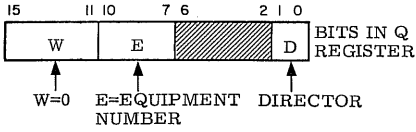
Bit in A Register	Meaning
A08	Mask 3
A07	Mask 2
A06	Mask 1
A05	Mask 0
A04	Not defined
A03	Reserve flag
A02	Not defined
A01	Not defined
A00	Interrupt on 1716 end of operation

STATUS RESPONSE

1716 Status

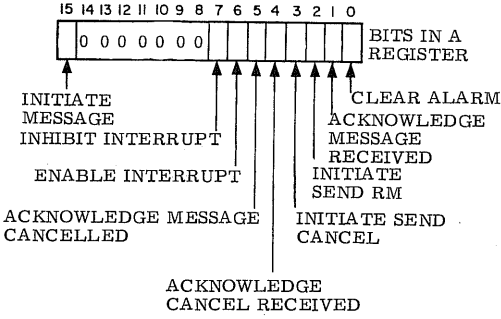


ADDRESSES

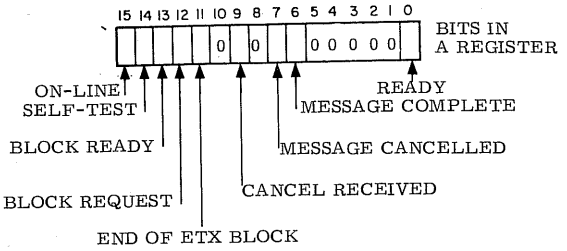


D	Computer Instruction	
	Output from A	Input to A
00	Output data	Input data
01	Function 1	Status 1
10		Status 2

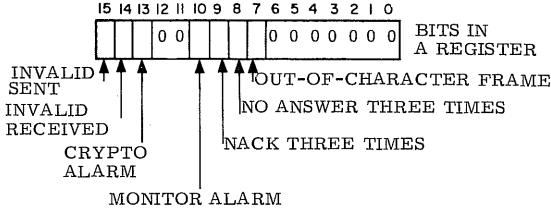
Director Function 1



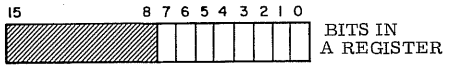
Status Word 1



Status Word 2



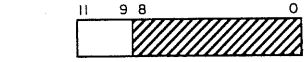
Data Words



1718-A SATELLITE COUPLER

DIVISION A

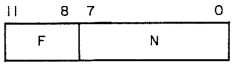
ADDRESSES



To connect division A, the 3000 Series computer channel transmits a 12-bit Connect code to the 1718. Division A must be connected before a data path is established between the computers, and the Connect code must match the switch setting on division A. Bits 9-11 are the significant bits in the Connect code; bits 0-8 are not used.

OPERATIONS

Functions



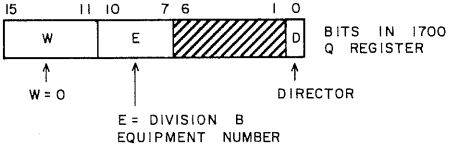
F	N	Description
0001	XXXXXXXX	Set flags for "1's" in N
0010	XXXXXXXX	Clear flags for "1's" in N
0100	XXXXXXXX	Set Mask register for "1's" in N
1000	XXXXXXXX	Clear Mask register for "1's" in N
0000	00000001	Select interrupt if other computer is not running
0000	00000010	Clear conditions set up by F = 0000, N = 00000001
0000	00000100	Select interrupt if other computer reads or writes
0000	00001000	Clear condition set up by F = 0000, N = 00000100

STATUS RESPONSE

Bit	Definition (Bit = "1")
11	Not Used
10	Division B Write
9	Division B Read
8	Division B Computer Running
7	Flag 7
6	Flag 6
5	Flag 5
4	Flag 4
3	Flag 3
2	Flag 2
1	Flag 1
0	Flag 0

DIVISION B

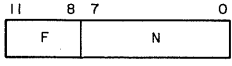
ADDRESSES



D	1704 Instruction	Division Operation
0	Output from A	Write data
0	Input to A	Read data
1	Output from A	Write function code
1	Input to A	Read status

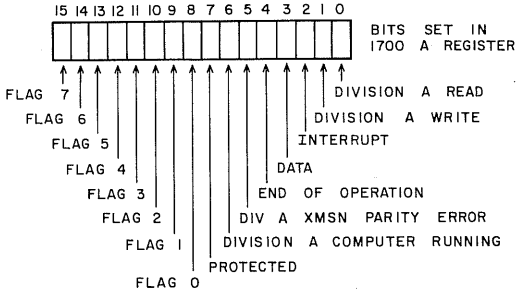
OPERATIONS

Functions



F	N	Description
0001	XXXXXXXX	Set flags for "1's" in N
0010	XXXXXXXX	Clear flags for "1's" in N
0100	XXXXXXXX	Set Mask register for "1's" in N
1000	XXXXXXXX	Clear Mask register for "1's" in N
0000	XXXXXXX1	Clear
0000	XXXXXX1X	Clear interrupt and 8-bit Character mode
0000	XXXXX1XX	Data interrupt request
0000	XXXX1XXX	End of operation interrupt request
0000	XXX1XXXX	Alarm interrupt request
0000	XX1XXXXX	Start input data transfer
0000	X1XXXXXX	Stop data transfer
0000	1XXXXXXX	Set 8-bit Character mode

STATUS RESPONSE



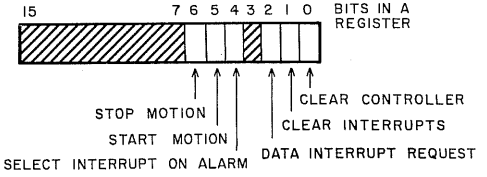
1721-A/B/C/D/1722-A/B PAPER TAPE READER

ADDRESSES

Q Register	Computer Instruction	
	Output From A	Input To A
00A0		Read
00A1	Director Function	Director Status

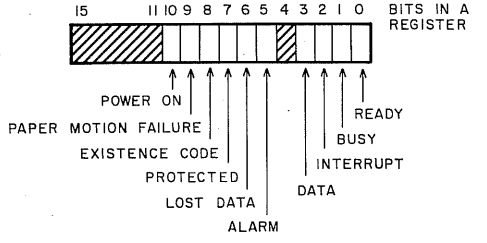
OPERATIONS

Director Function



STATUS RESPONSE

Director Status



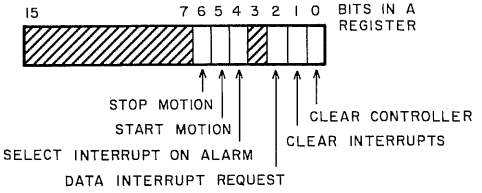
1723-A/B/1724-A/B PAPER TAPE PUNCH

ADDRESSES

Q Register	Computer Instruction	
	Output From A	Input To A
00C0	Write	
00C1	Director Function	Director Status

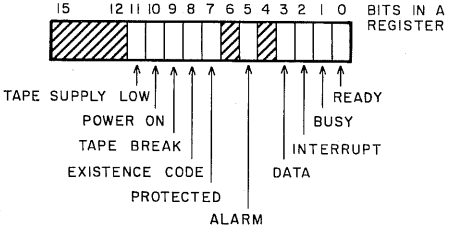
OPERATIONS

Director Function



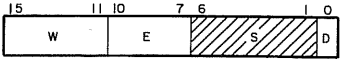
STATUS RESPONSE

Director Status



1726 CARD READER CONTROLLER

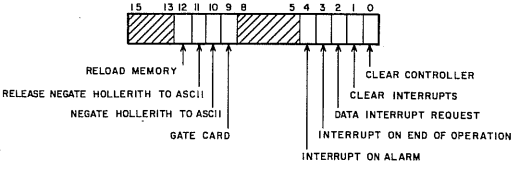
ADDRESS



D (Q Bit 00)	With Signal	Instruction	Operation
0	Read or Write	Output From A	Data Transfer
1	Write	Output From A	Director Function
1	Read	Input To A	Director Status

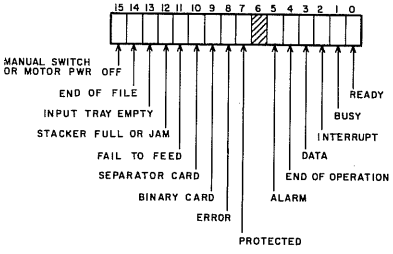
OPERATIONS

Director Function

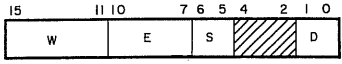


STATUS RESPONSE

Director Status



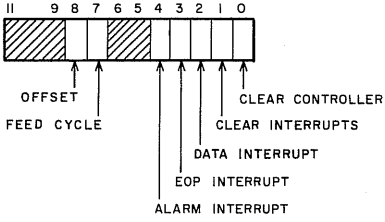
ADDRESS



D Q Bits 00	01	S Q Bits 05	06	With Signal	Instruction	Operation
0	0	1	0	Read	Input To A	Data Transfer (Reader)
0	0	0	1	Write	Output From A	Data Transfer (Punch)*
1	0	0 or 1	0 or 1	Write	Output From A	Director Function
1	0			Read	Input To A	Director Status (Level 1)
1	1			Read	Input To A	Director Status (Level 2)

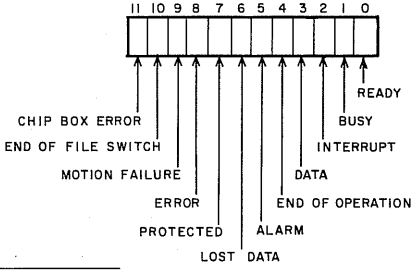
OPERATIONS

Director Function



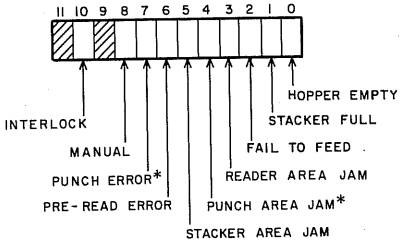
STATUS RESPONSE

Director Status Level 1



*1728 only

Director Status Level 2



*1728 only

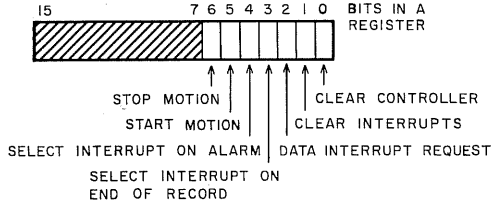
1729-A/B CARD READER

ADDRESSES

Q Register	Computer Instruction	
	Output From A	Input To A
00E0		Read
00E1	Director Function	Director Status

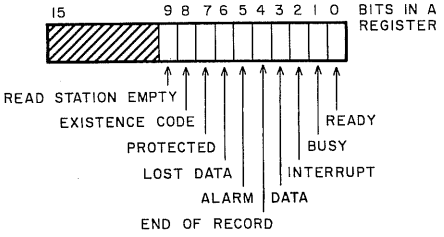
OPERATIONS

Director Function

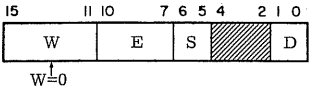


STATUS RESPONSE

Director Status:



ADDRESS

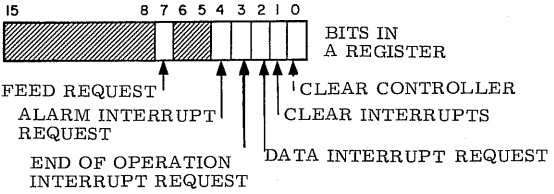


D Q Bits		S Q Bits		Instruction	
00	01	05	06	Output from A	Input to A
0	0	1	0	Director Function	Data Transfer
1	0	1	0		Director Status 1
1	1	1	0		Director Status 2

Data transfers to A00 through A11 with data read from las
column. A00 corresponds to card row 9.

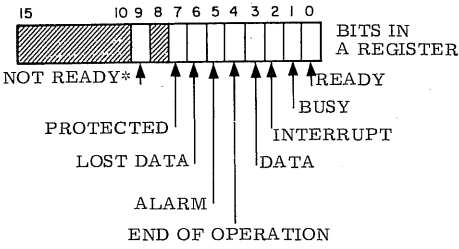
OPERATIONS

Director Function



STATUS RESPONSE

Director Status 1



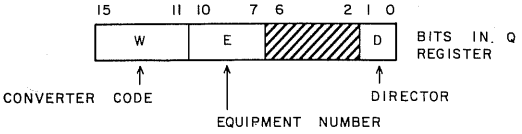
Director Status 2

Transfers 0000_{16} to the A register.

*Always Inverse of Bit 00

1731-A/B MAGNETIC TAPE CONTROLLER

ADDRESSES

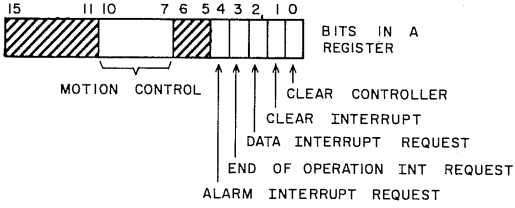


E (Bits 10-7 of Q)	Equipment Number	E (Bits 10-7 of Q)	Equipment Number
0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	B
0100	4	1100	C
0101	5	1101	D
0110	6	1110	E
0111	7	1111	F

	Computer Instruction	
D	Output From A	Input To A
00	Write	Read
01	Control Function	Director Status 1
10	Unit Select	Director Status 2

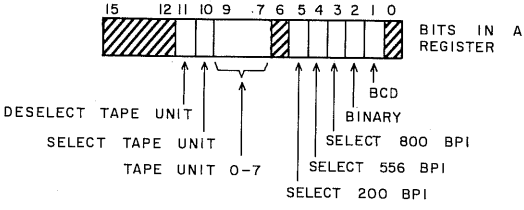
OPERATIONS

Control Function



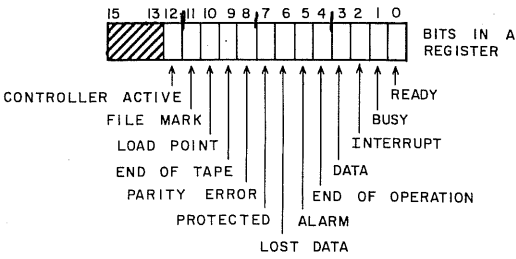
Bits 10-7 of A	Motion Function
0001	Write Motion
0010	Read Motion
0011	Backspace
0101	Write File Mark
1000	Rewind Load
1100	Rewind Unload

Unit Select

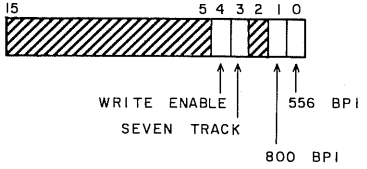


STATUS RESPONSE

Director Status 1



Director Status 2



1732-A/B MAGNETIC TAPE CONTROLLER

ADDRESSES

Same as for the 1731-A/B Magnetic Tape Controller.

OPERATIONS

Same as for the 1731-A/B Magnetic Tape Controller, with the following differences:

Control Function

Bits 10 - 7 of A	Motion Function
0001	Write motion
0010	Read motion
0011	Backspace
0101	Write file mark/tape mark
0110	Search file mark/tape mark forward
0111	Search file mark/tape mark backward
1000	Rewind load
1100	Rewind unload

Unit Select

The following additional bits in the A register are used:

Bit 0 = Character mode
Bit 6 = Assembly/disassembly

STATUS RESPONSE

Director Status 1

Same as for the 1731-A/B Magnetic Tape Controller with the addition of bit 13 at the A register, which indicates Fill.

Directory Status 2

Same as for the 1731-A/B Magnetic Tape Controller.

1732-2 MAGNETIC TAPE CONTROLLER

ADDRESSES

Same as for the 1731-A/B Magnetic Tape Controller.

OPERATIONS

Same as for 1732-A/B Magnetic Tape Controller with the following exception:

D Field	Output from A	Input to A
11	Buffered Input/Output	Current Address

Unit Select

Bit 5 of A register = Select 1600 bpi.

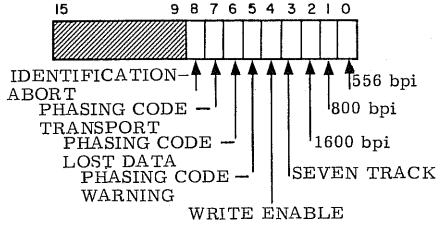
STATUS RESPONSE

Director Status 1

Same as for 1732-A/B Magnetic Tape Controller with the addition of the following:

Bit 14 = Storage parity error
Bit 15 = Protect fault

Directory Status 2



Current Address

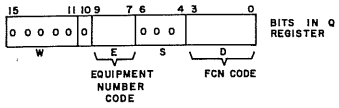
Loads the A register with the address of the next word to be transferred.

NEW MOTION FUNCTIONS

The following table shows the time in which a New Motion must be initiated to achieve nonstop motion at maximum speed after an EOP status/interrupt.

KTT - SPEED	t (t-msec)		
	Write Forward	Read Forward	Read Reverse
37.5 ips	2.7 msec	2.0 msec	2.7 msec
75 ips	1.3 msec	1.0 msec	1.3 msec
Alternative for next control function	1. Write Motion 2. Write File Mark/ Tape Mark	1. Read Motion 2. Search File Mark/ Tape Mark	1. Backspace 2. Search File Mark/Tape Mark Backward

ADDRESS

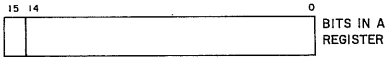


D	Computer Instruction	
	Output From A	Input to A
0000	Core to core normal*	
1000	Core to core reverse*	
0001	Director function	Controller status
0010	Load address A/Q	File address status
1010	Load address DSA	
0011	Write	Current word address status*
0100	Read	
0101	Compare	
0110	Checkword check, from address in A register	
1110	Checkword check, from current address	
0111	Write address	

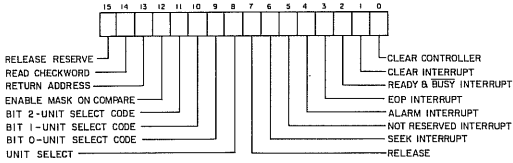
*These functions will be rejected if CDC Special Option 60141-1 is not installed.

OPERATIONS

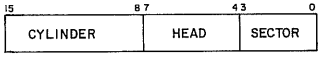
Core to Core Normal or Core to Core Reverse



Director Function

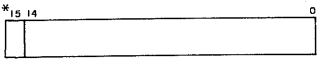


Load Address A/Q, Load Address DSA, Write Address, or File Address Status

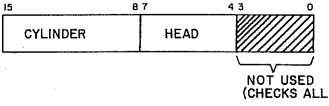


*Bit 15 is used when 65K memory is available.

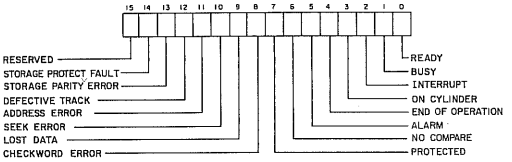
Write, Read, or Compare



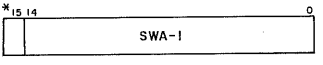
Checkword Check, From Address in A Register or
Checkword Check, From Current Address



Controller Status



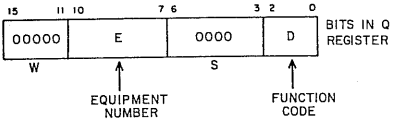
Current Word Address Status



*Bit 15 is used when 65K memory is available.

1733-2 CARTRIDGE DISK DRIVE CONTROLLER

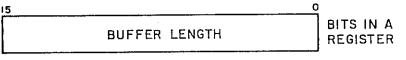
ADDRESS



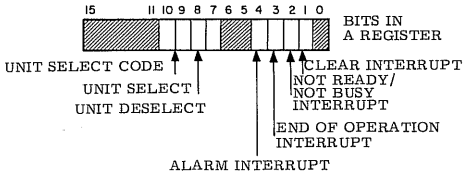
	Computer Instruction	
D	Output From A	Input To A
000	Load Buffer	Clear Controller
001	Director Function	Director Status
010	Load Address	Cylinder Address Status
011	Write	Current Word Address Status
100	Read	Checkword Status
101	Compare	Drive Cylinder Status
110	Checkword Check	
111	Write Address	

OPERATIONS

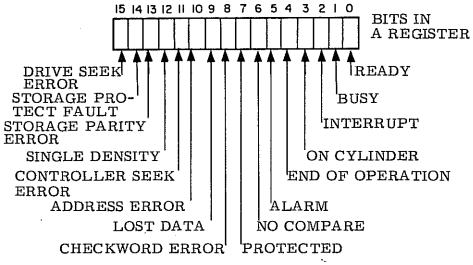
Load Buffer



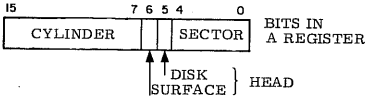
Director Function



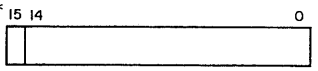
Director Status



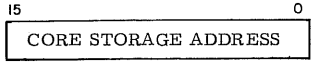
Load Address Function, Cylinder Address Status



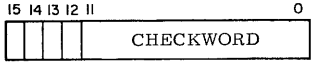
Write, Read, Compare



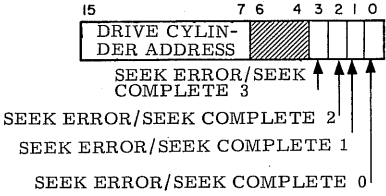
Current Word Address Status



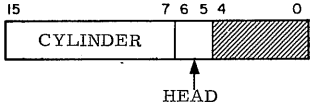
Checkword Status



Drive Cylinder Status

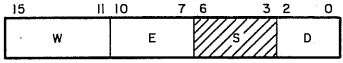


Checkword Check, Write Address Functions



*Bit 15 is used only with 65K mode.

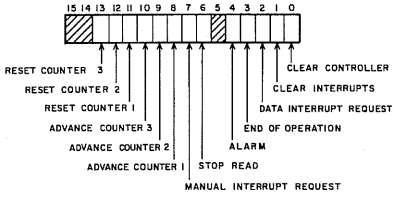
ADDRESS



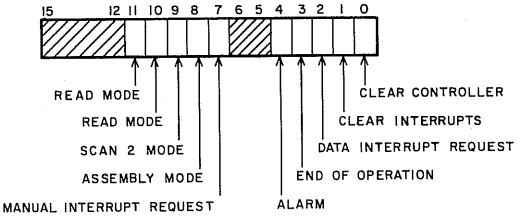
D (Q Bits 02-00)	INSTRUCTION	OPERATION
000	Input To A	Data Input Mode
001	Output From A	Operating Mode
001	Input To A	Equipment Status Mode
010	Output From A	Data Mode
010	Input To A	Mirror Status Mode
011	Output From A	Positioning Mode
100	Output From A	Mechanical Action Mode
101	Output From A	Initiate Read Mode

OPERATIONS

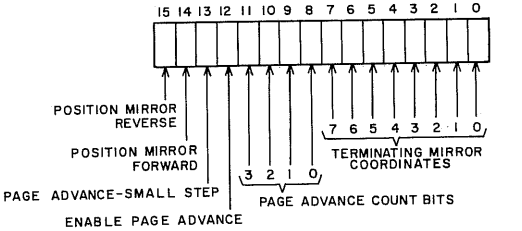
Operating Mode (D = 1)



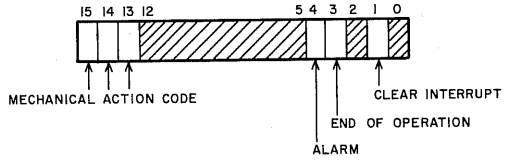
Data Mode (D = 2)



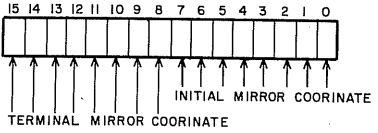
Positioning Mode (D = 3)



Mechanical Mode (D = 4)

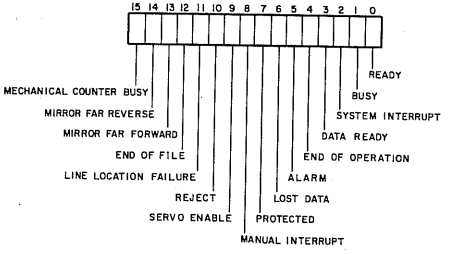


Initiate Read Mode (D = 5)

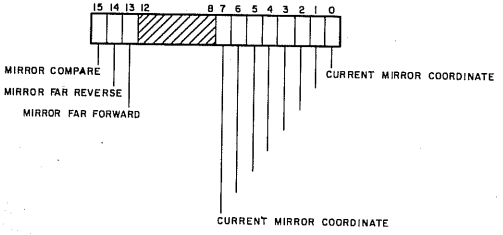


STATUS RESPONSE

Director Status 1

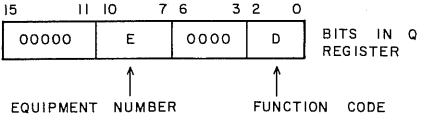


Director Status 2



1738-A/B DISK PACK CONTROLLER

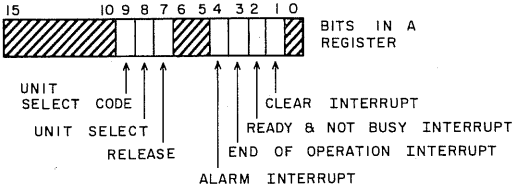
ADDRESSES



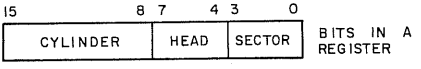
	Computer Instruction	
D	Output From A	Input To A
001	Director Function	Director Status
010	Load Address	Address Register Status
011	Write	
100	Read	
101	Compare	
110	Checkword Check	
111	Write Address	

OPERATIONS

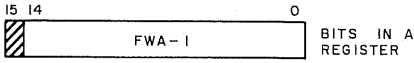
Director Function



Load Address , Checkword Check, Write Address or Address Register Status

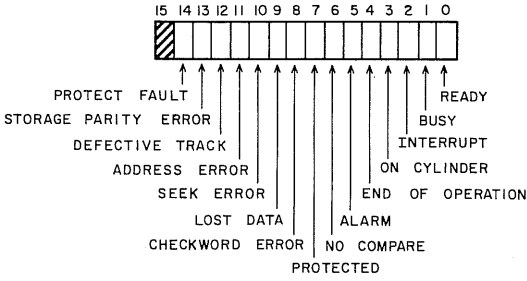


Write, Read, or Compare

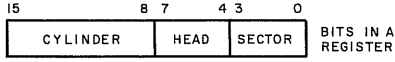


STATUS RESPONSE

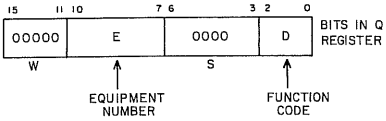
Director Status



Address Register Status



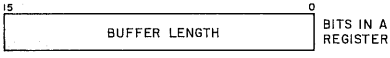
ADDRESS



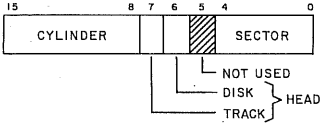
	Computer Instruction	
D	Output From A	Input To A
000	Load Buffer	Clear Controller
001	Director Function	Director Status
010	Load Address	Cylinder Address Status
011	Write	Current Word Address Status
100	Read	Checkword Status
101	Compare	Drive Cylinder Status
110	Checkword Check	
111	Write Address	

OPERATIONS

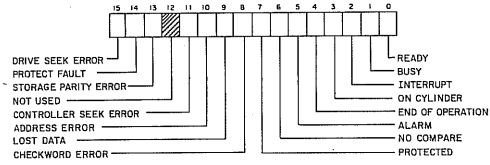
Load Buffer



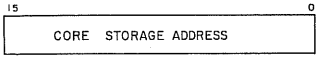
Write Address, Cylinder Address Status



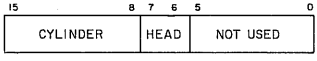
Director Status



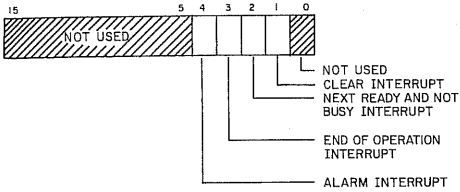
Current Word Address Status



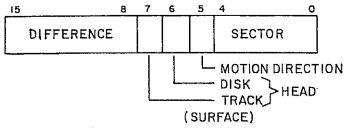
Checkword Check



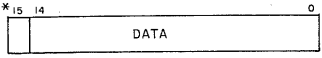
Director Function



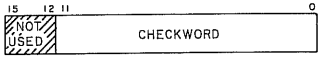
Load Address



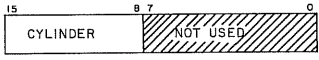
Write, Read, Compare



Checkword Status



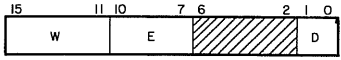
Drive Cylinder Status



*Used for 65K memory.

1740 LINE PRINTER CONTROLLER

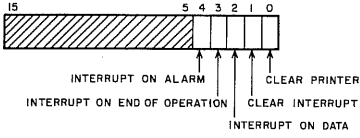
ADDRESS



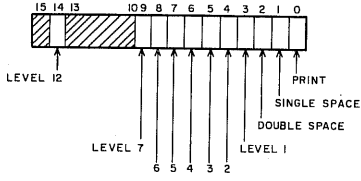
(Q BITS 01-00)	INSTRUCTION	OPERATION
00	Output From A	Data Transfer
01	Output From A	Director Function 1
11	Output From A	Director Function 2
11	Input To A	Director Status

OPERATIONS

Director Function 1

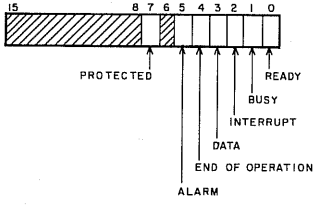


Director Function 2



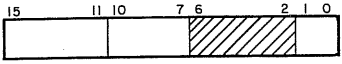
STATUS RESPONSE

Director Status



1742-A/B LINE PRINTER

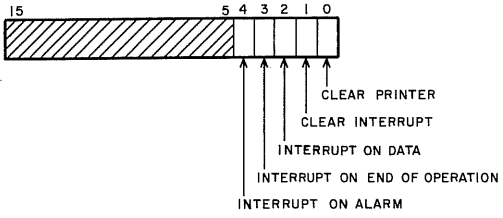
ADDRESS



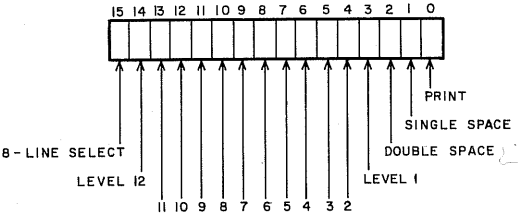
D (Q Bits 01-00)	INSTRUCTION	OPERATION
00 01 11	Data Transfer Director Function 1 Director Function 2	 Director Status

OPERATIONS

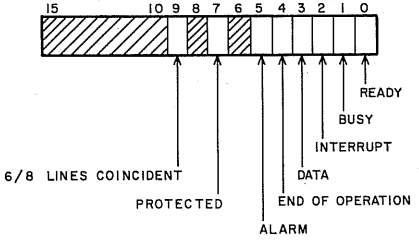
Director Function 1



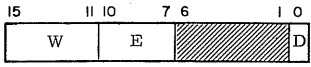
Director Function 2



STATUS RESPONSE
Director Status



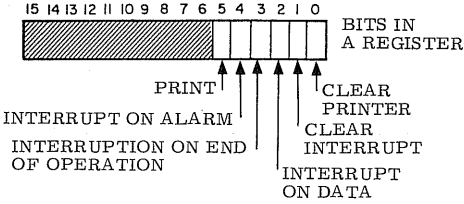
ADDRESS



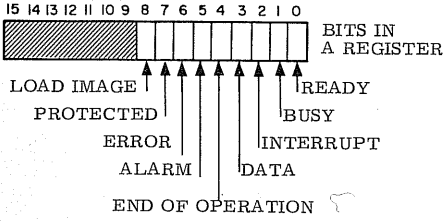
D	Instruction	
Q BIT 0	Input to A	Output from A
0	Illegal	Data Transfer
1	Director Status	Director Function

OPERATIONS

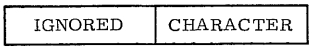
Director Function



Director Status



Data Transfer



FORMAT CONTROL CHARACTER

The first character of each line is defined as the control character and is not printed.

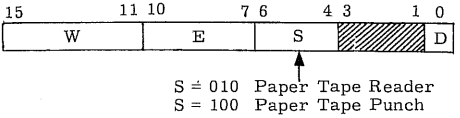
CONTROL CHARACTER FUNCTIONS

Function	Bits in A Register					
	A05	A04	A03	A02	A01	A00
Suppress Space	0	X	X	X	0	0
Single Space	0	X	X	X	0	1
Double Space	0	X	X	X	1	0
Triple Space	0	X	X	X	1	1
Vertical Format Control						
Channel 1	1	X	0	0	0	0
Channel 2	1	X	0	0	0	1
Channel 3	1	X	0	0	1	0
Channel 4	1	X	0	0	1	1
Channel 5	1	X	0	1	0	0
Channel 6	1	X	0	1	0	1
Channel 7	1	X	0	1	1	0
Channel 8	1	X	0	1	1	1
Channel 9	1	X	1	0	0	0
Channel 10	1	X	1	0	0	1
Channel 11	1	X	1	0	1	0
Channel 12	1	X	1	0	1	1
Illegal as vertical format controls	1	X	1	1	0	0
	1	X	1	1	0	1
	1	X	1	1	1	0
	1	X	1	1	1	1

Note: When an illegal vertical control is issued, the character is decoded as if A05 were set to 0.

1777-1/1777—2 PAPER TAPE STATION

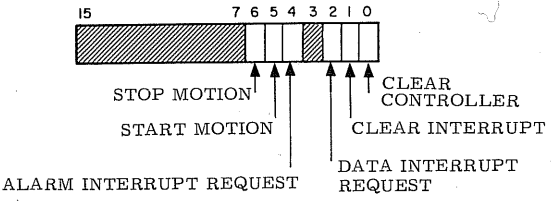
ADDRESS



D	Computer Instructions	
	Output from A	Input to A
0	Write Function	Read Status
1		

OPERATIONS

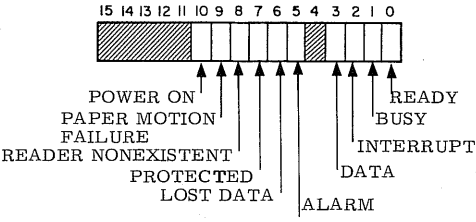
Director Function



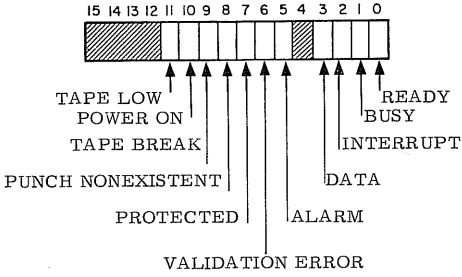
STATUS RESPONSE

Director Status

If the S field is set to 010, the following is the status for the paper tape reader:



If the S field is set to 100, the following is the status for the paper tape punch:



1779 CHARACTER HANDLING

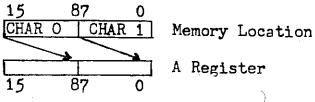
This feature is available on the 1774 only. It provides Character Addressing of memory on Load A and Store A instructions from the lower character position of the A register to the lower or upper character position of the Memory Location.

Enable Character Addressing (ECA) = 0580
Disable Character Addressing (DCA) = 05C0

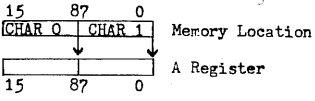
Bit 0 of the i register controls which character is selected, it is called the Character Designation Bit (CDB).

Load A (LDA)

CDB = 0

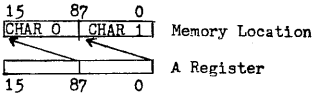


CDB = 1

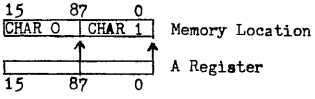


Store A (STA)

CDB = 0



CDB = 1



BINARY-DECIMAL-HEXADECIMAL RELATIONSHIPS

DECIMAL	HEXADECIMAL	BINARY
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

LITHO IN U.S.A.

CONTROL DATA
CORPORATION

CORPORATE HEADQUARTERS, 8100 34th AVE. SO., MINNEAPOLIS, MINN. 55440
SALES OFFICES AND SERVICE CENTERS IN MAJOR CITIES THROUGHOUT THE WORLD